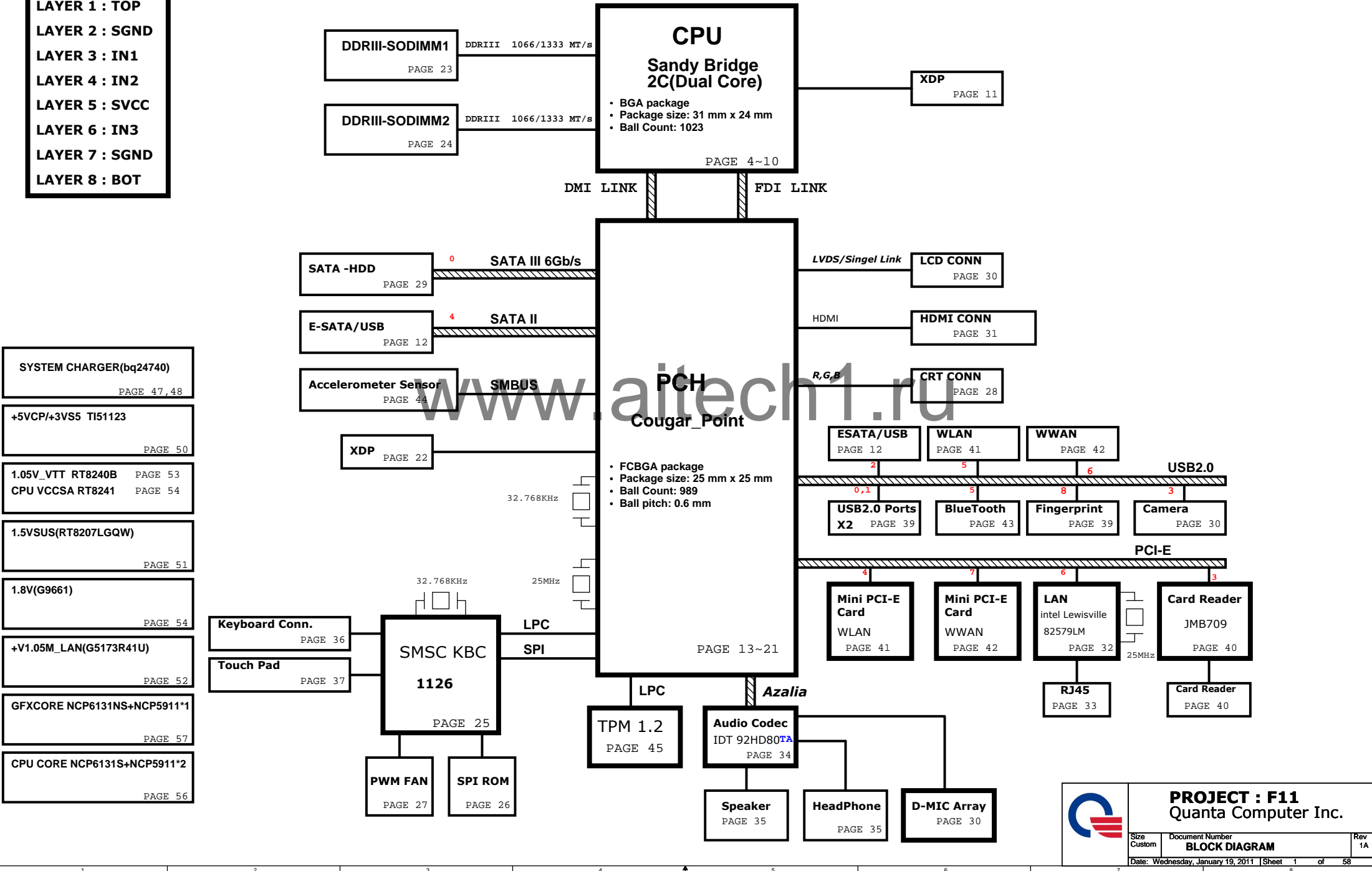


# PCB STACK UP

## 8L UMA. PV

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : SVCC  
LAYER 6 : IN3  
LAYER 7 : SGND  
LAYER 8 : BOT

# F11, Foreigner (Huron River) BLOCK DIAGRAM 01



power State	+RTC_CELL	+VIN +3VPCU	+3VS5 +5VS5	+5VSUS +1.5VSUS	+5V +3V +1.8V_GFX +1.8V +1.5V +1.5V_CPU +1.1V_VTT +1.05V +1.0V_GFX +VGA_CORE +VCORE
S0	ON	ON	ON	ON	ON
S1	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4/S5 AC	ON	ON	ON	OFF	OFF
S4/S5 DC Only	ON	ON	OFF	OFF	OFF
AC/DC No Exist	ON	OFF	OFF	OFF	OFF

PCIE	Foreigner
1	X
2	X
3	JMB709
4	WLAN
5	X
6	NIC
7	WWAN
8	X

SATA	Foreigner
0	HDD
1	X
2	X
3	X
4	eSATA
5	X

USB	Foreigner
0	CONN(USB Charger)
1	CONN
2	eSATA
3	CAMERA
4	X
5	BT or WLAN
6	X
7	X
8	Finger print
9	WWAN
10	X
11	X
12	X
13	X

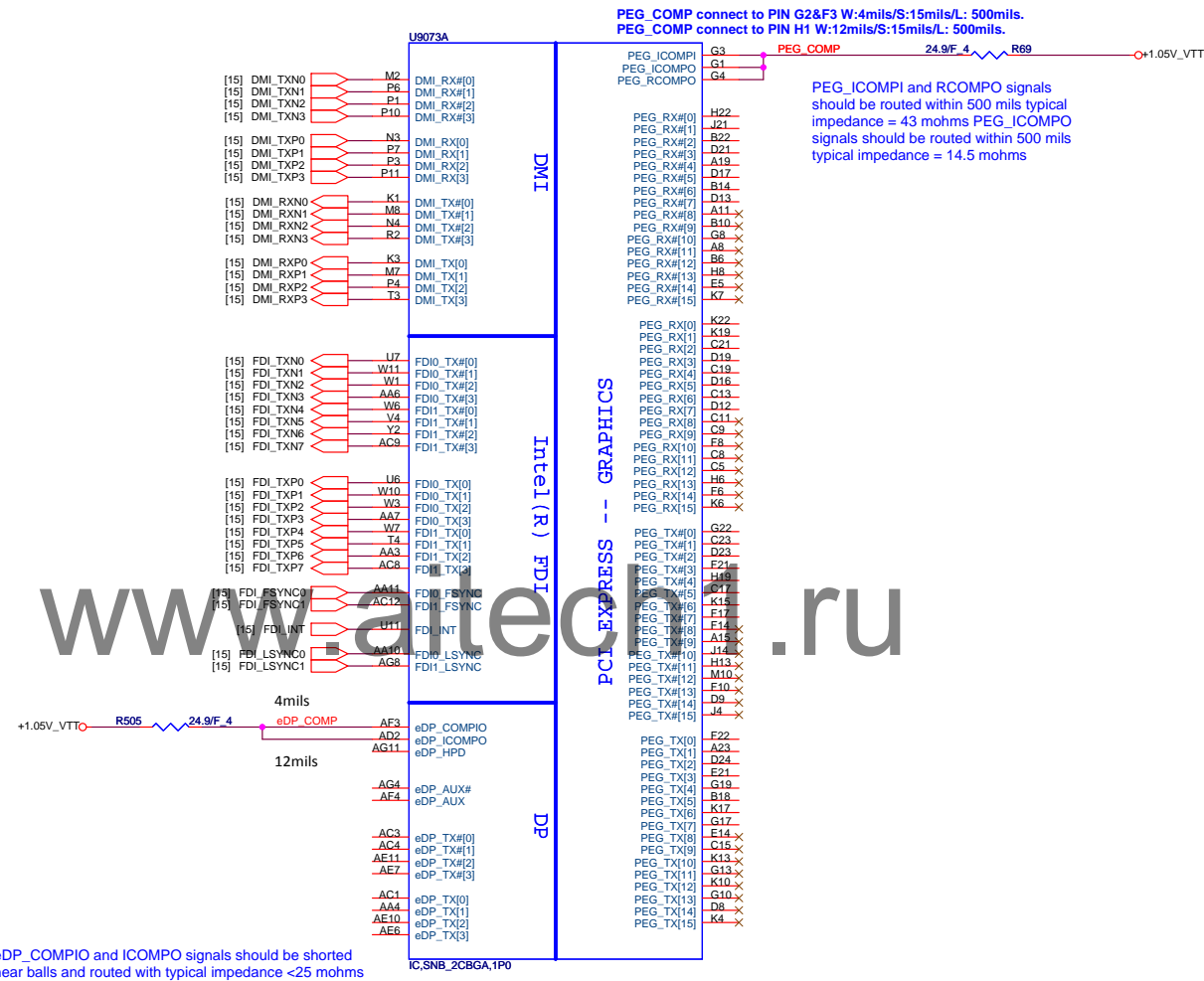
	SOURCE	BATTERY 0x16	CLK GEN 0xD2	Thermal IC 0x98(Write) / 0x99(Read)	G-SENSOR 0x3A(Write) / 0x3B(Read)	WLAN	SO-DIMM DIMM0: 0xA0 DIMM1: 0xA4	SMSC 1126	Intel Lan Gbe PHY:0x64 Gbe MAC:0x70
SMB_PCH_CLK SMB_PCH_DAT	PCH	X	Y	Y	Y	Y	Y	X	X
SMB_ME0_CLK SMB_ME0_DAT	PCH	X	X	X	X	X	X	Y	Y
AB1A_CLK AB1A_DATA	SMSC 1126	Y	X	X	X	X	X	X	X



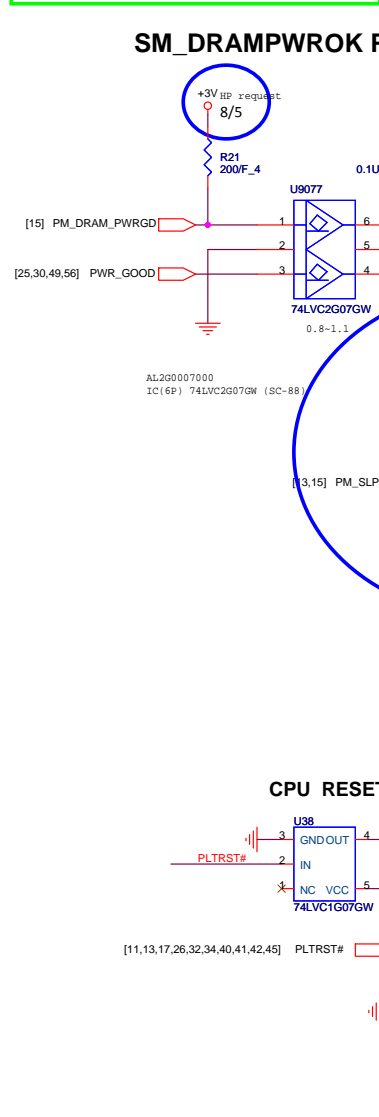
**PROJECT : F11**  
Quanta Computer Inc.



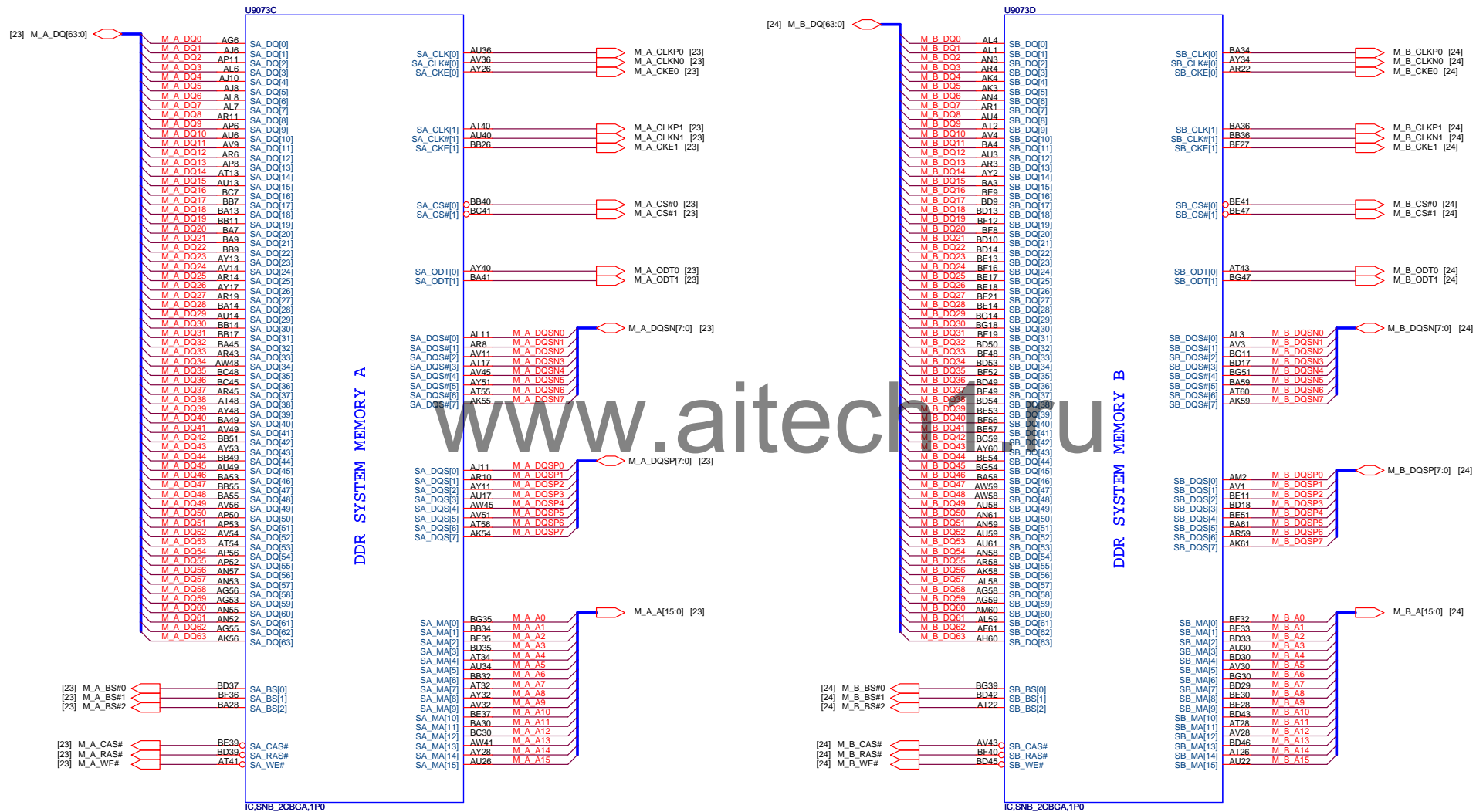
## Sandy Bridge Processor (DMI, PEG, FDI)

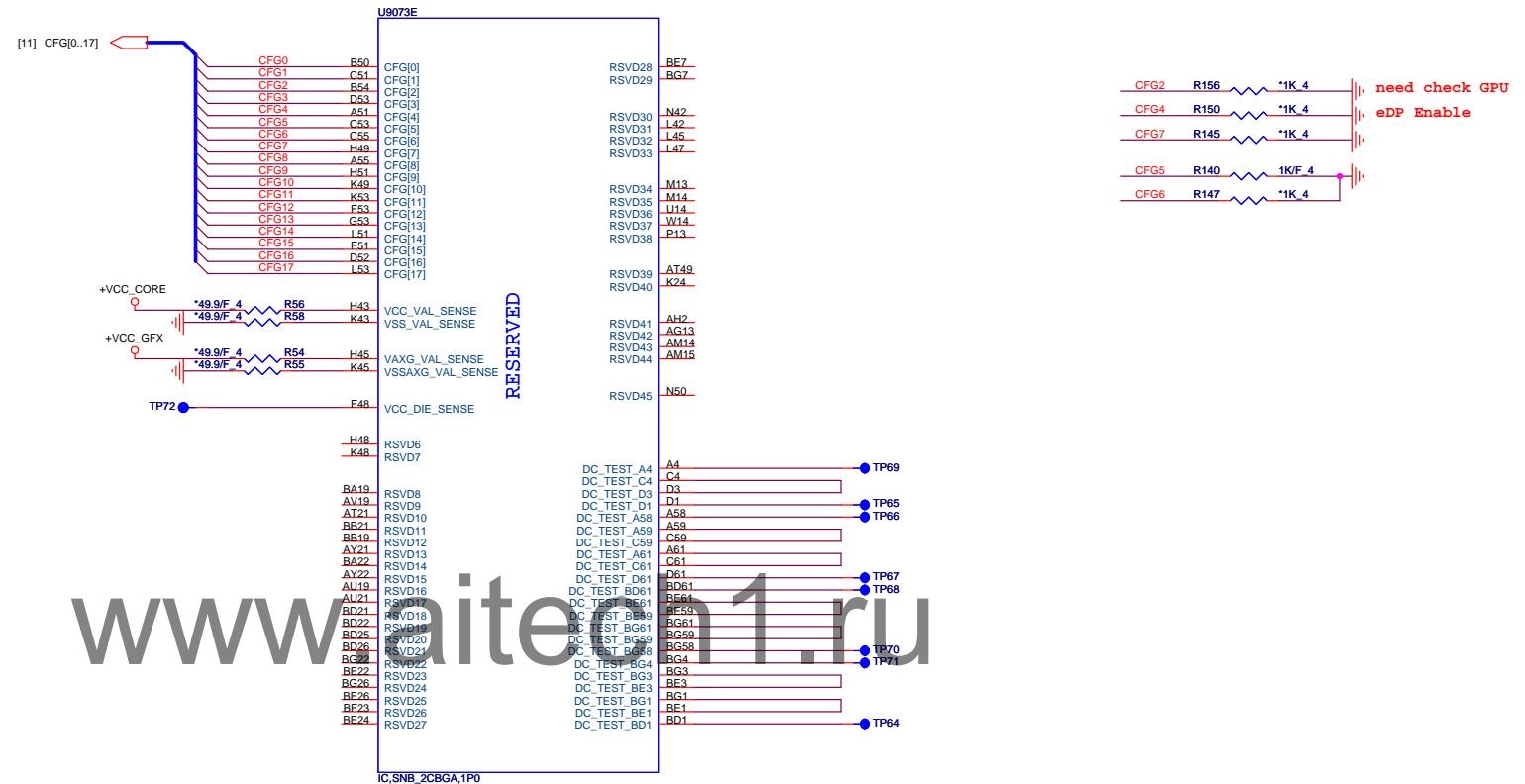


eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



## Sandy Bridge Processor (DDR3)





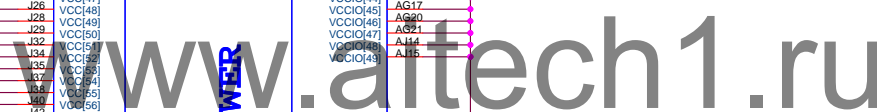
#### CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled  
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

#### Processor Strapping

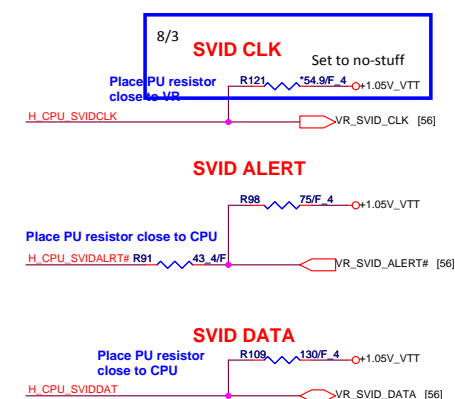
The CFG signals have a default value of '1' if not terminated on the board.

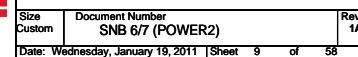
	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

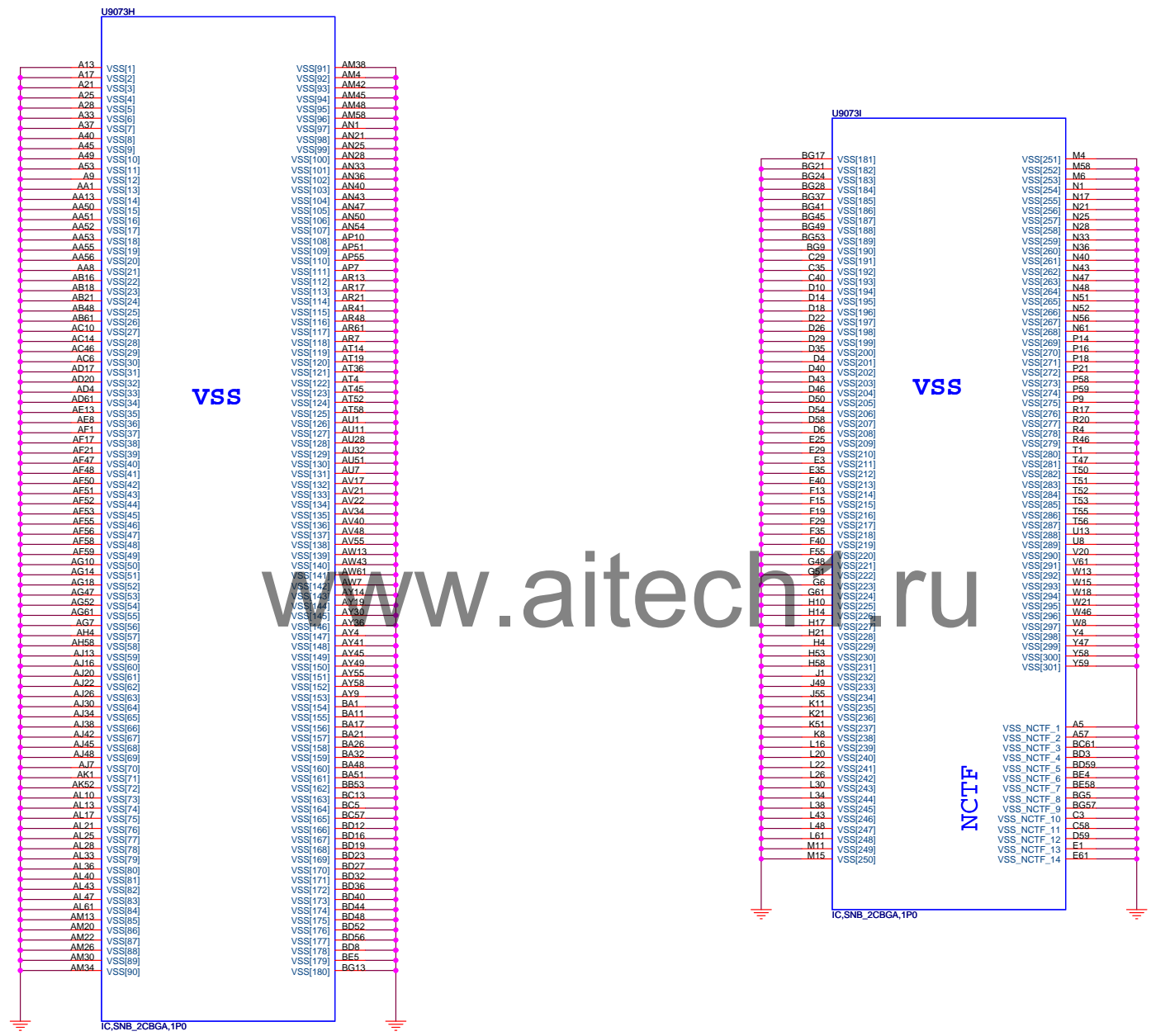


330uf \*4

330uf \*2

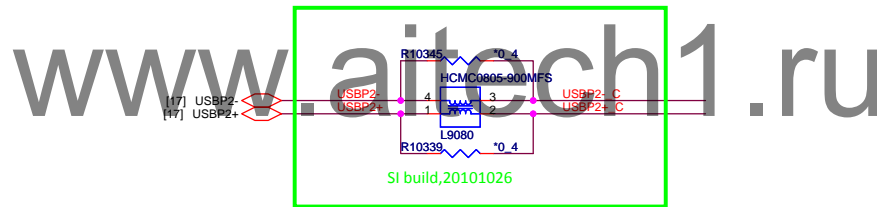
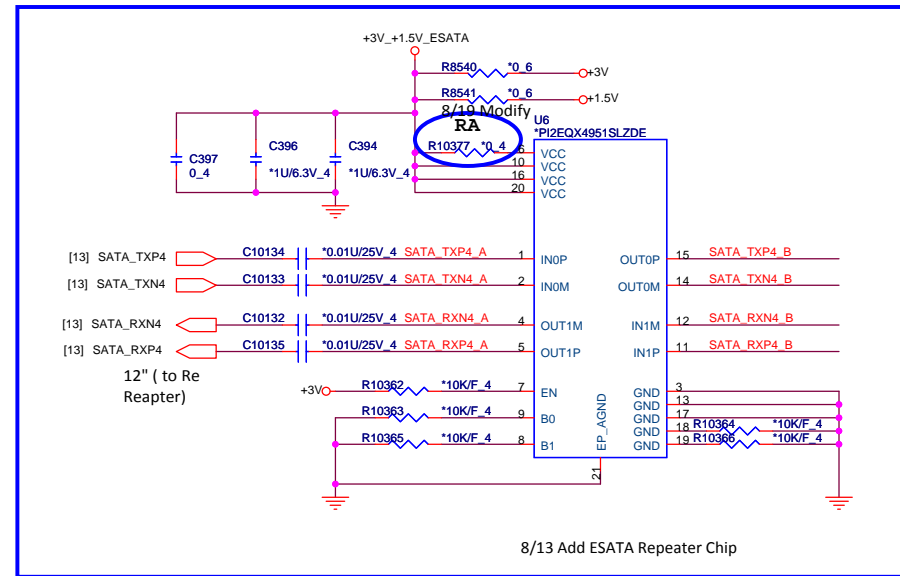




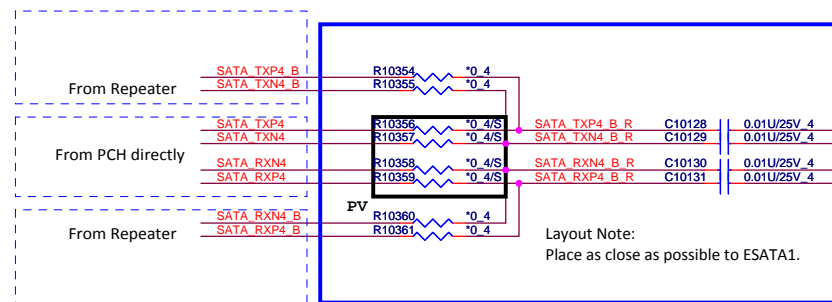
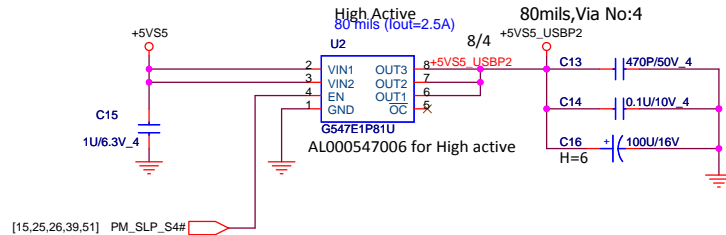




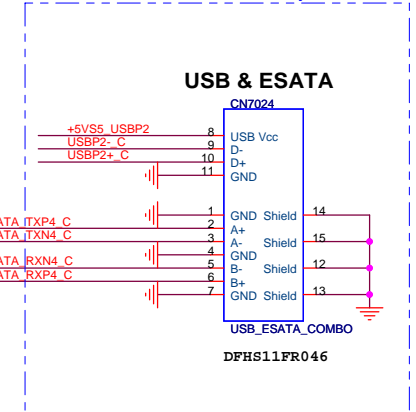
Signals		2EQX4951SL	3EQX4951ST
U6#6	RA	0 ohm	NC



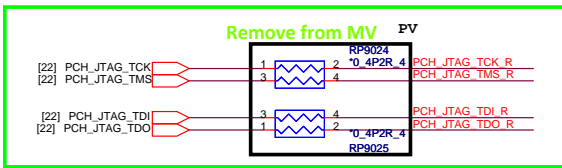
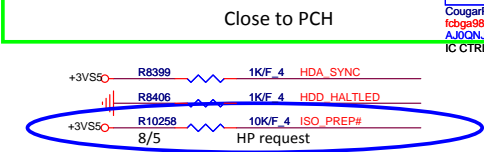
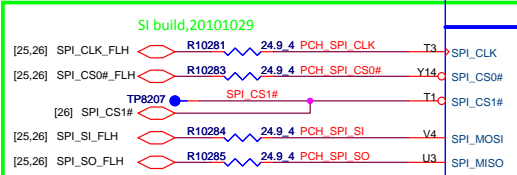
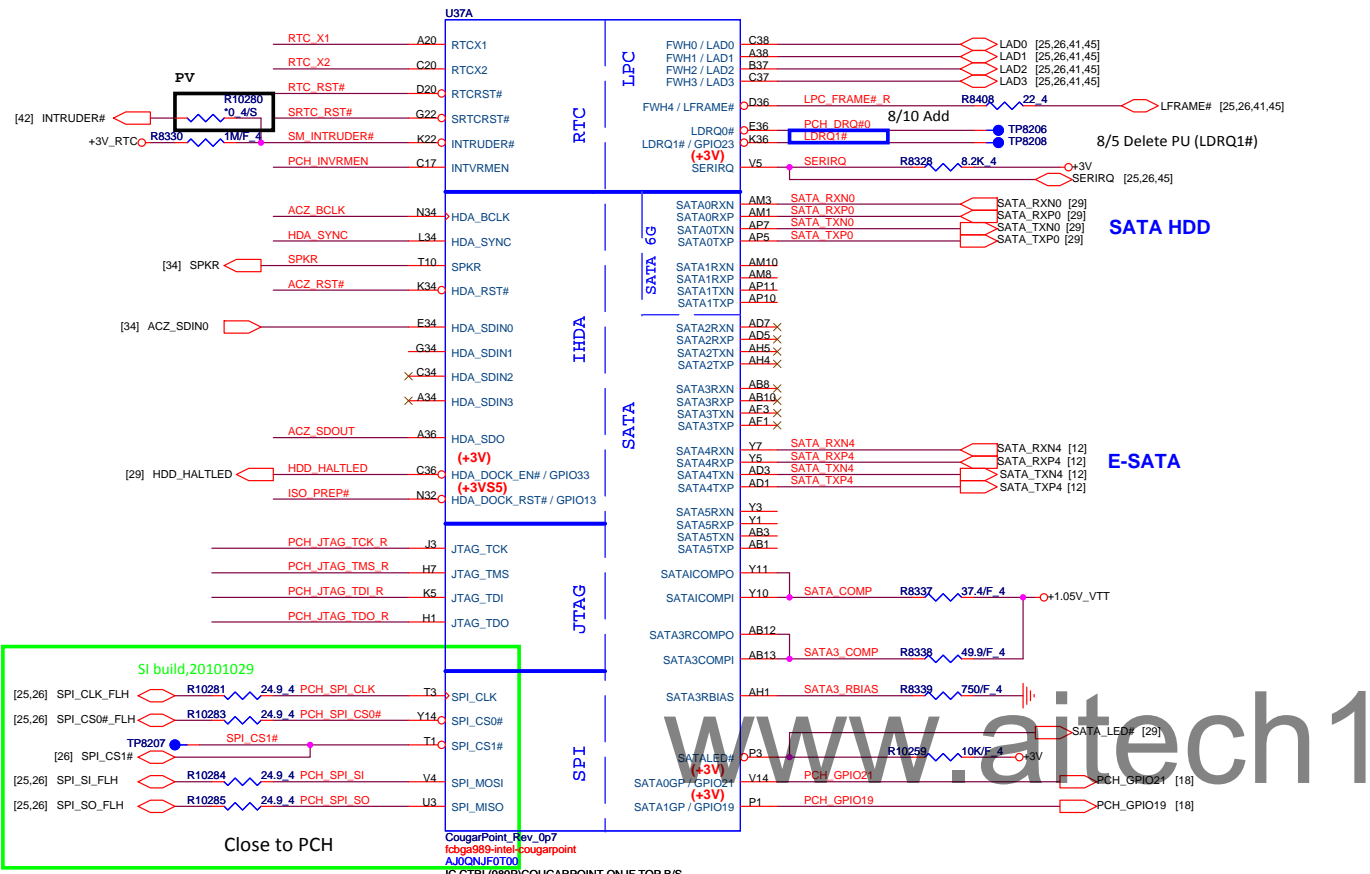
## Standard USB



## 8/25 Modify



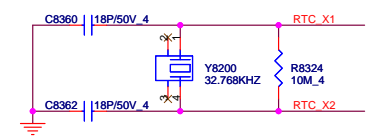
# Cougar Point (HDA,JTAG,SATA)



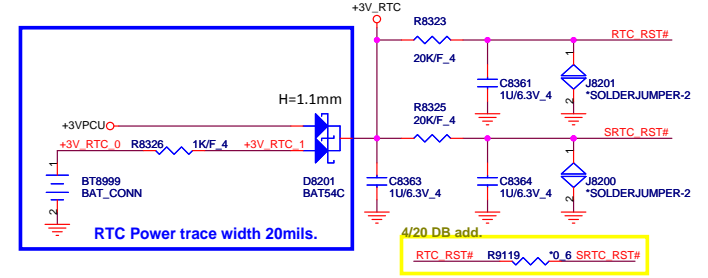
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R8348 1K 4 +3V
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R8351 330K/F 4 +3V_RTC
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R8359 1K 4 NV_ALE [17]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R8360 2.2K 4 R8361 4.7K/F 4 NV_CLE [17] H_SNB_IVB# [5]
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	SPI_SI_FLH R8398 1K/F 4 +3V

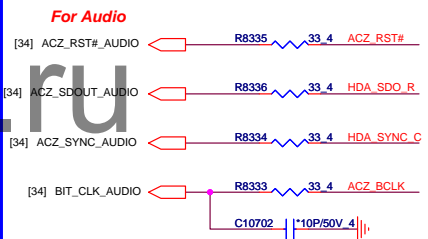
## RTC Clock 32.768KHz



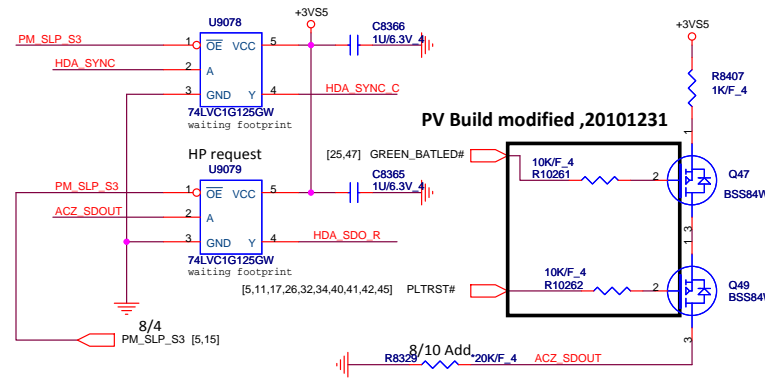
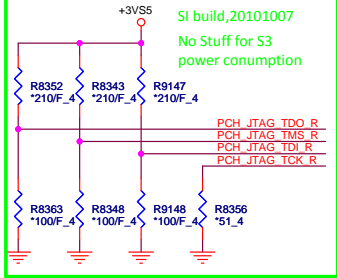
## RTC Circuitry(RTC)



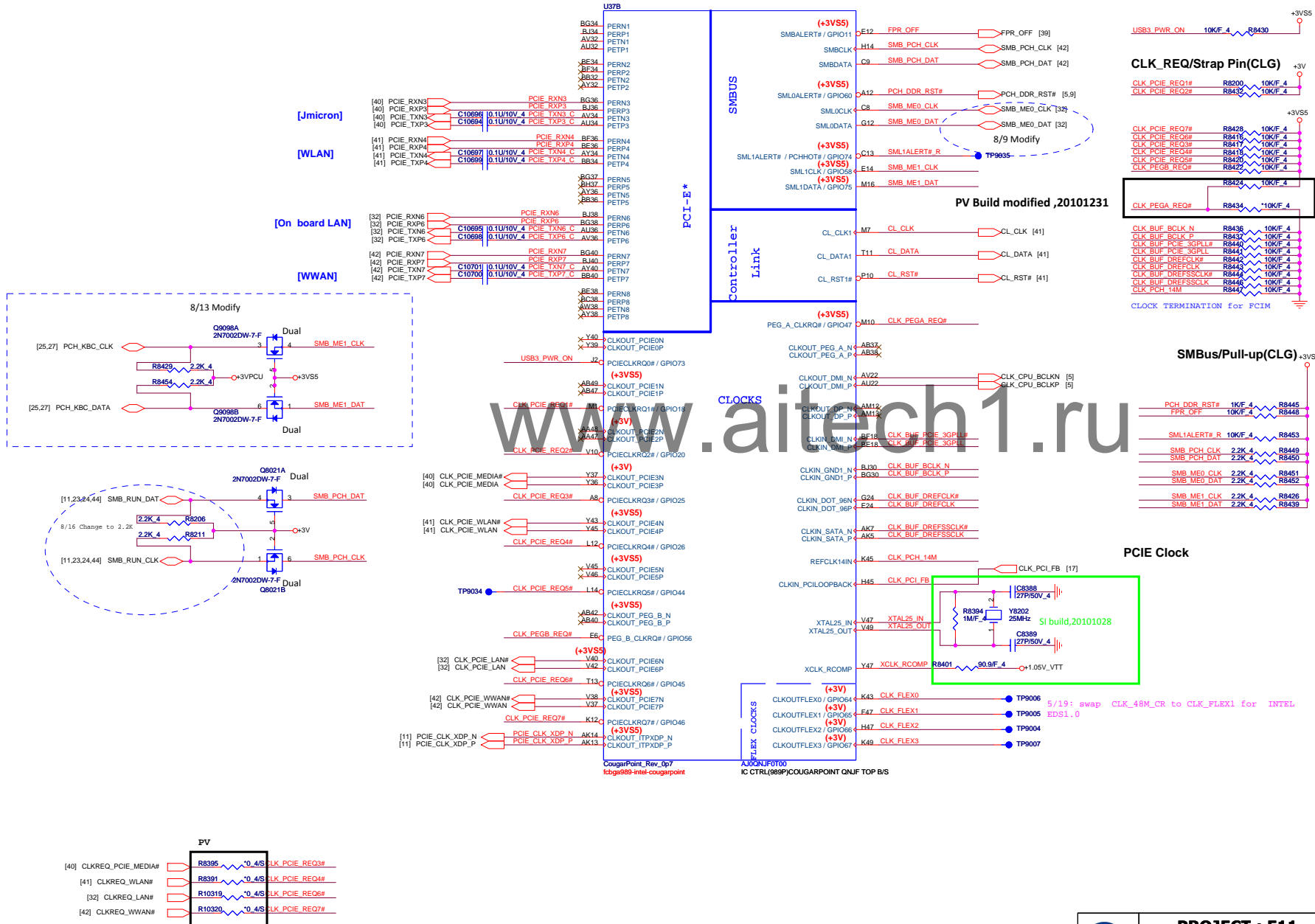
## HDA Bus(CLG)

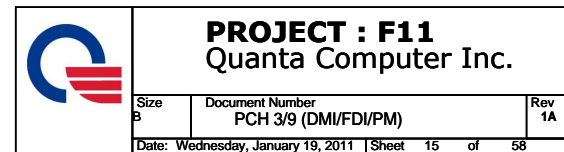


## PCH JTAG Debug(CLG)



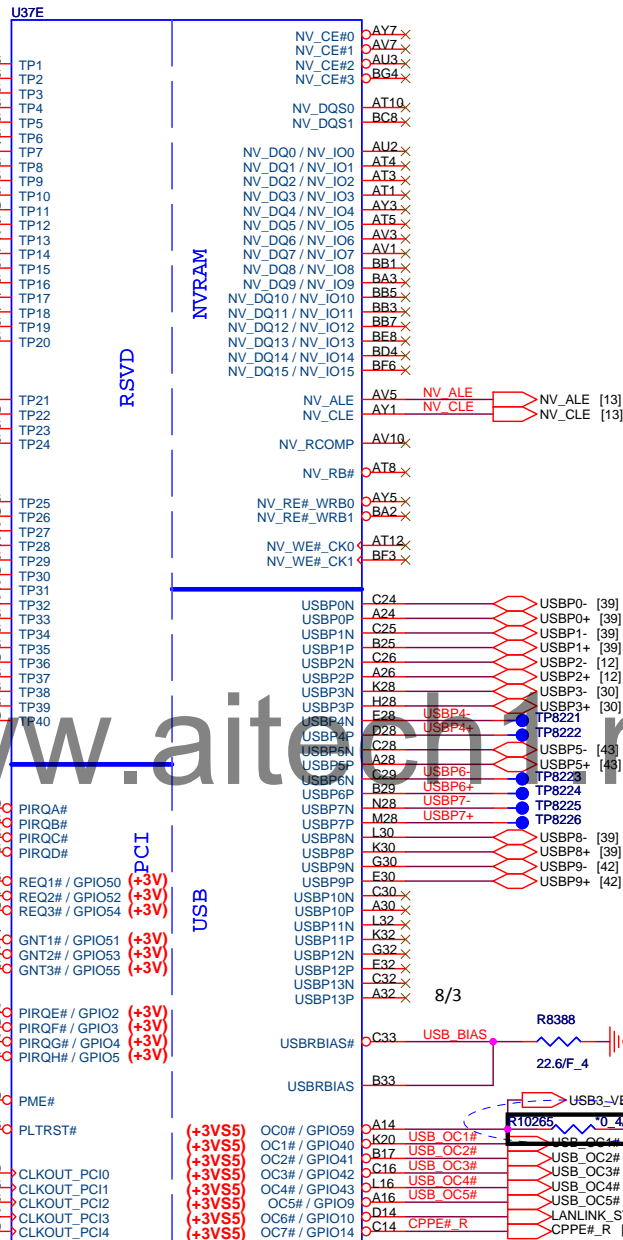
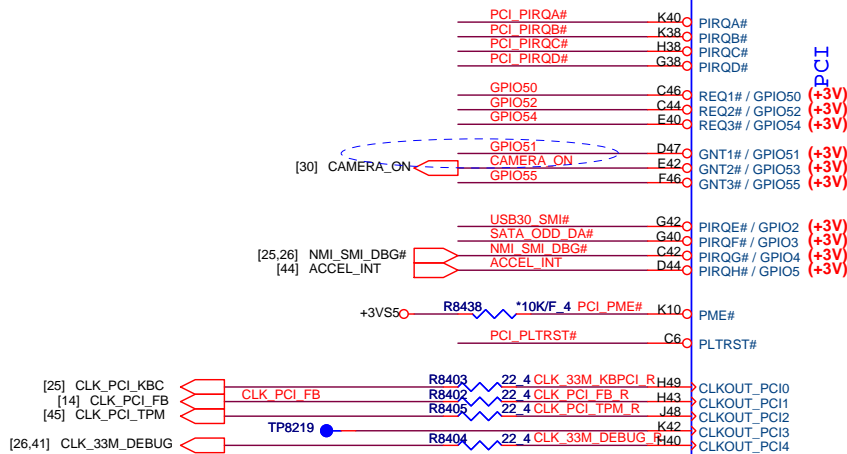
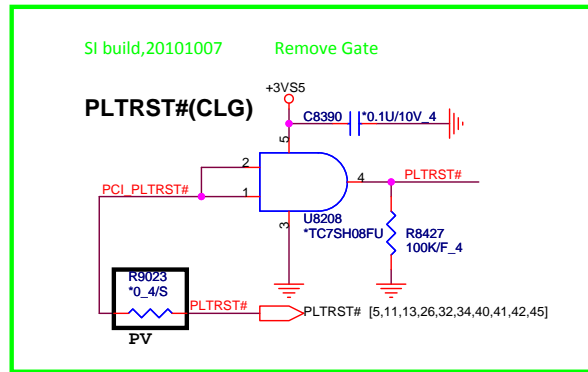
Cougar Point-M (PCI-E,SMBUS,CLK)



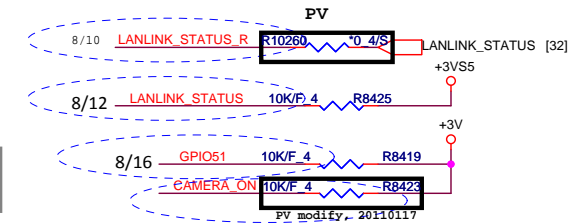
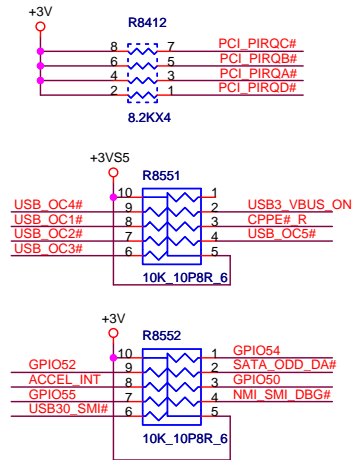




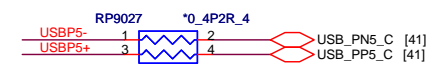
Size B	Document Number PCH 4/9 (LVDS/DDP/CRT)	Rev 1A
Date: Wednesday, January 19, 2011		Sheet 16 of 58



## PCI/USBOC# Pull-up(CLG)



## WLAN/BT Option

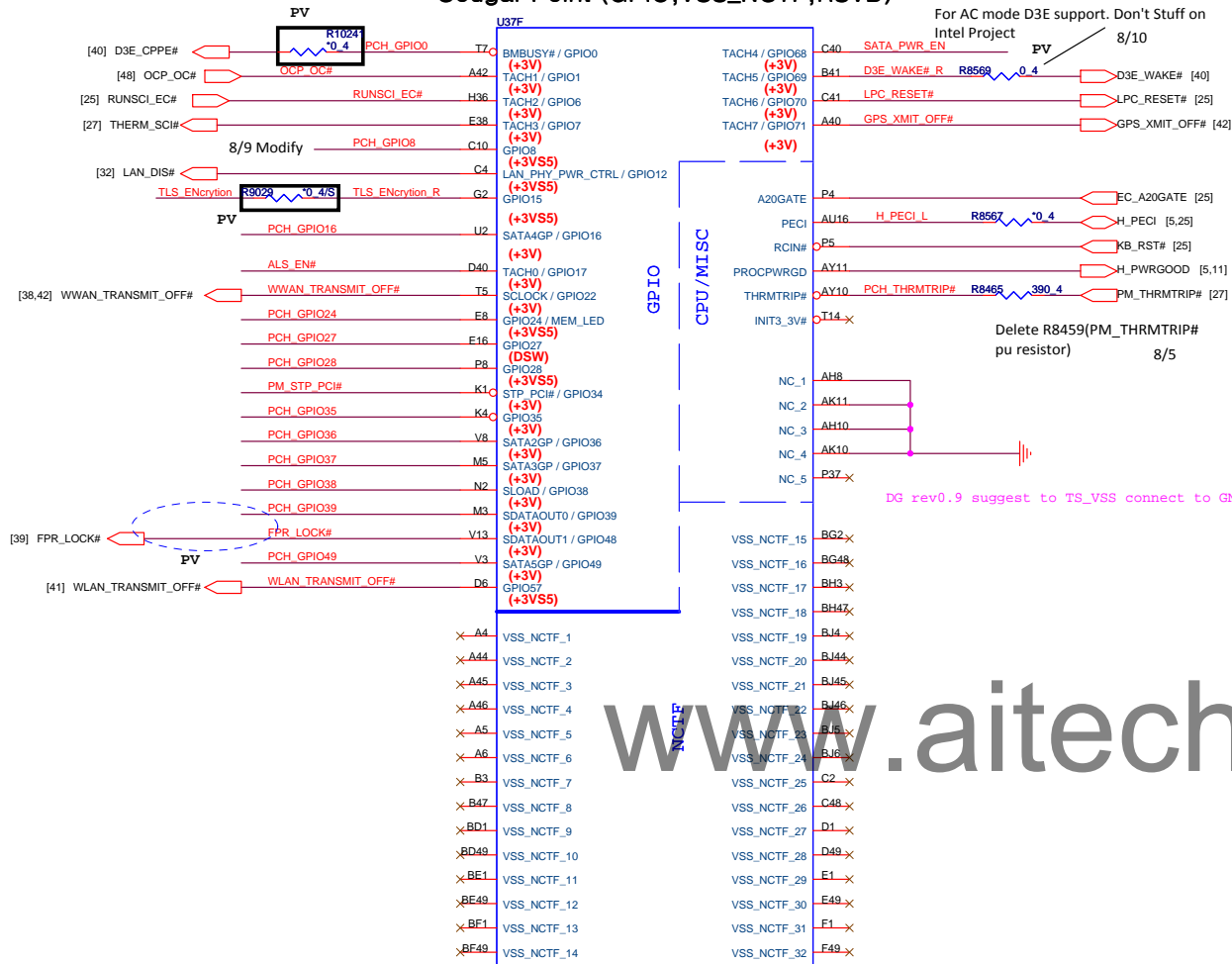


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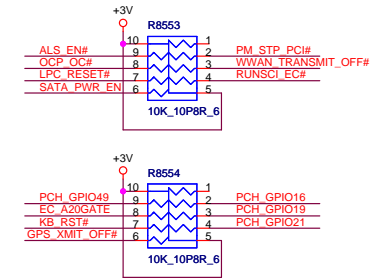
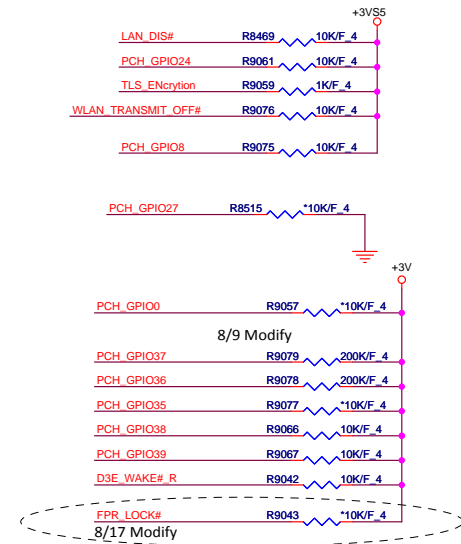
Size	Document Number	Rev
B	PCH 5/9 (PCI/USB/NVM)	1A
Date: Wednesday, January 19, 2011 Sheet 17 of 58		

CougarPoint\_Rev\_0p7  
fcbga989-intel-cougarpoint  
AJQNJF0100  
IC CTRL(989P)COUGARPOINT QNJF TOP B/S

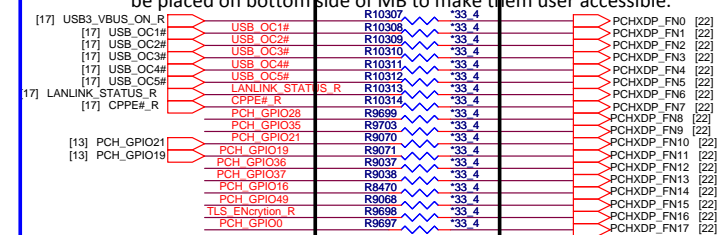
## Cougar Point (GPIO,VSS\_NCTF,RSVD)



## GPIO Pull-up/Pull-down(CLG)



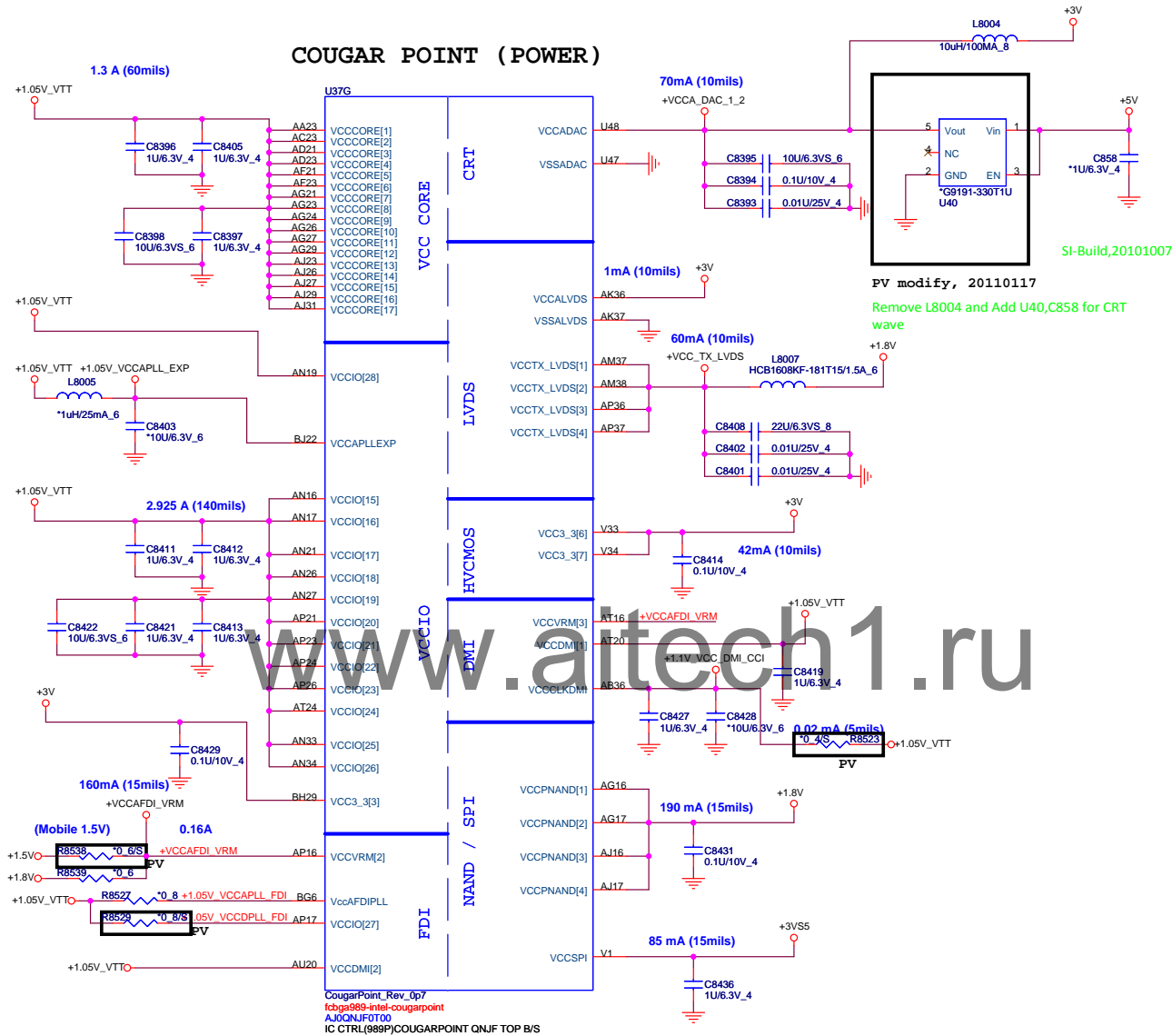
Layout note: 33 and 0 ohm related to XDP connector should be placed in close proximity to each other. In addition, these should be placed on bottom side of MB to make them user accessible.



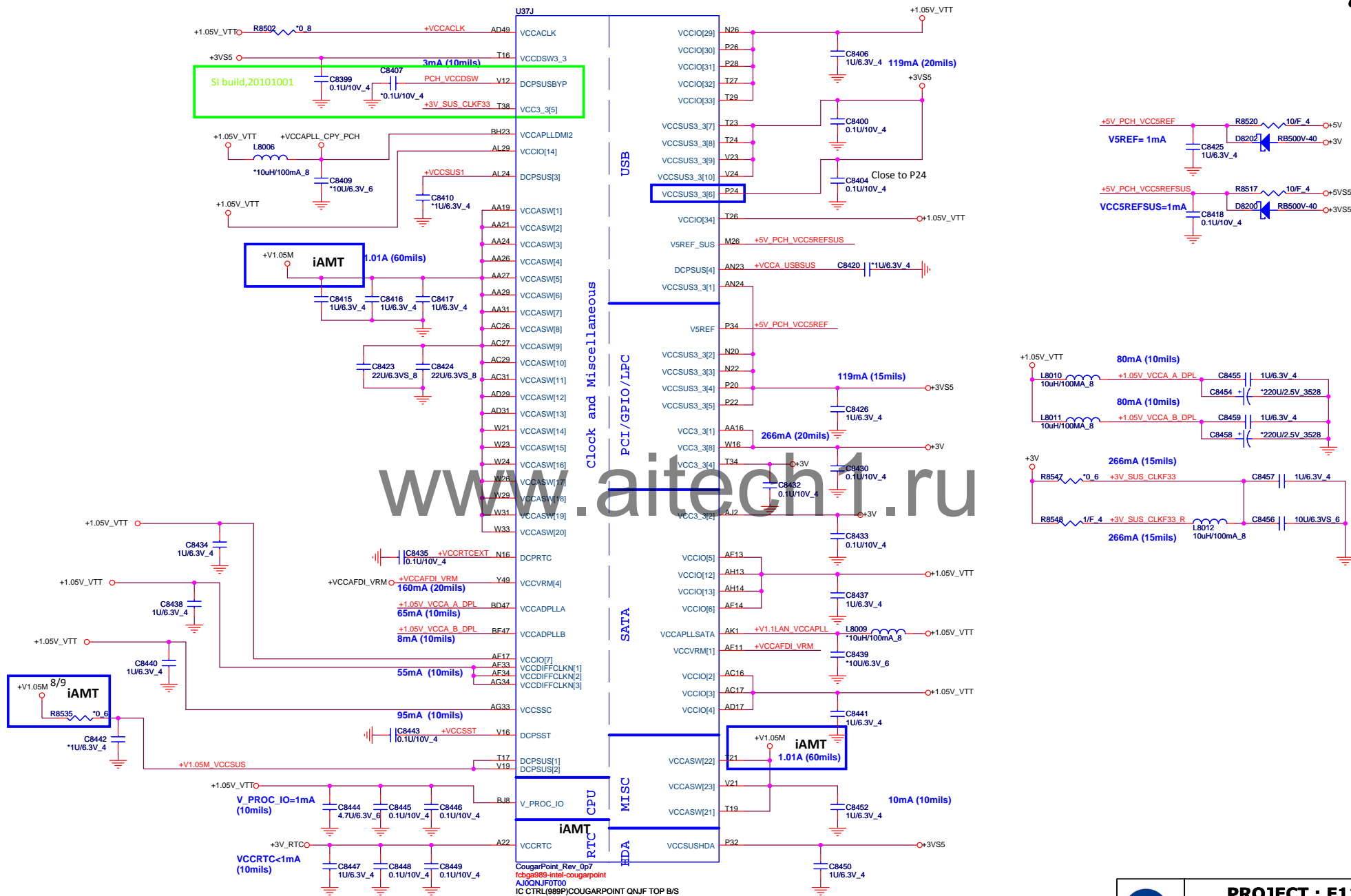
**PROJECT : F11**  
Quanta Computer Inc.

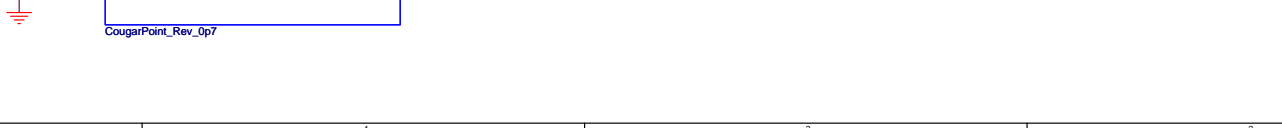
Size	Document Number	Rev
Custom	PCH 6/9 (GPIO/RSVD)	1A
Date: Wednesday, January 19, 2011	Sheet 18 of 58	

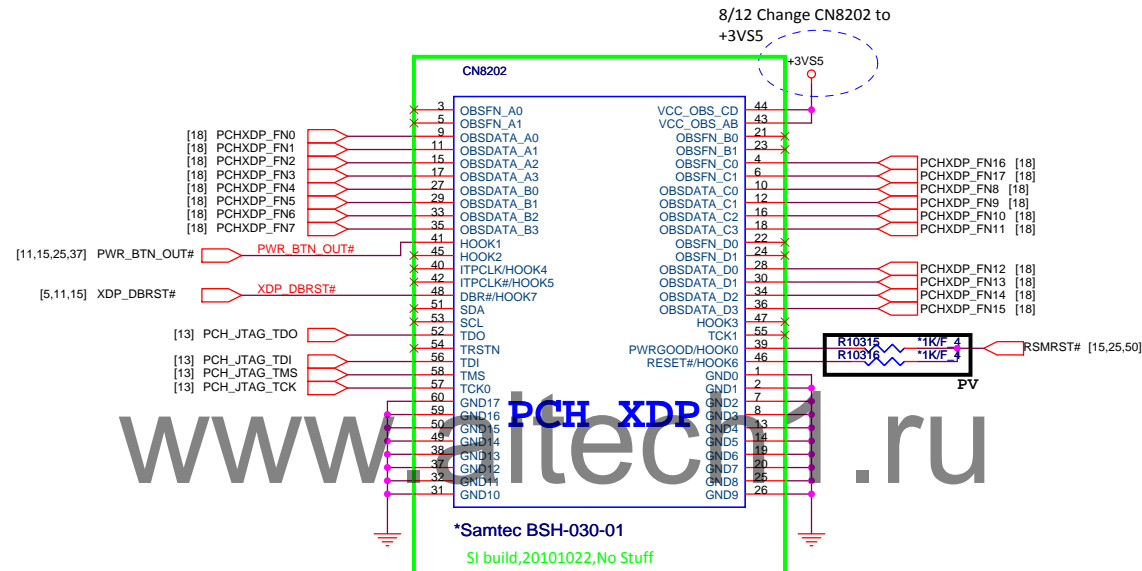
## COUGAR POINT (POWER)

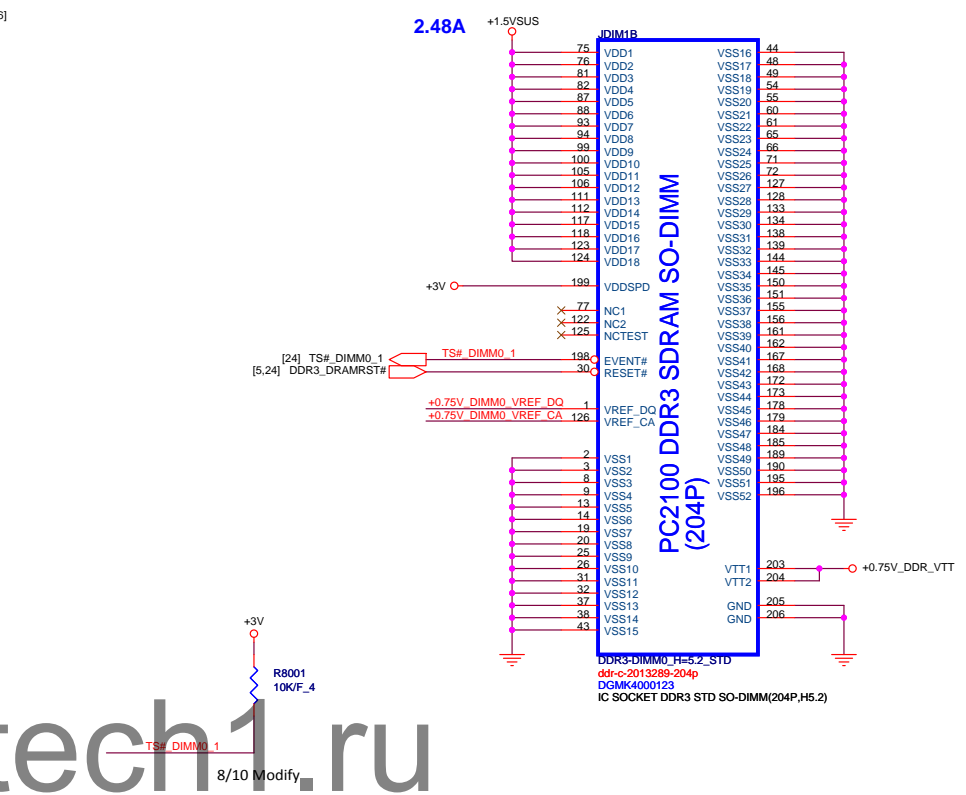
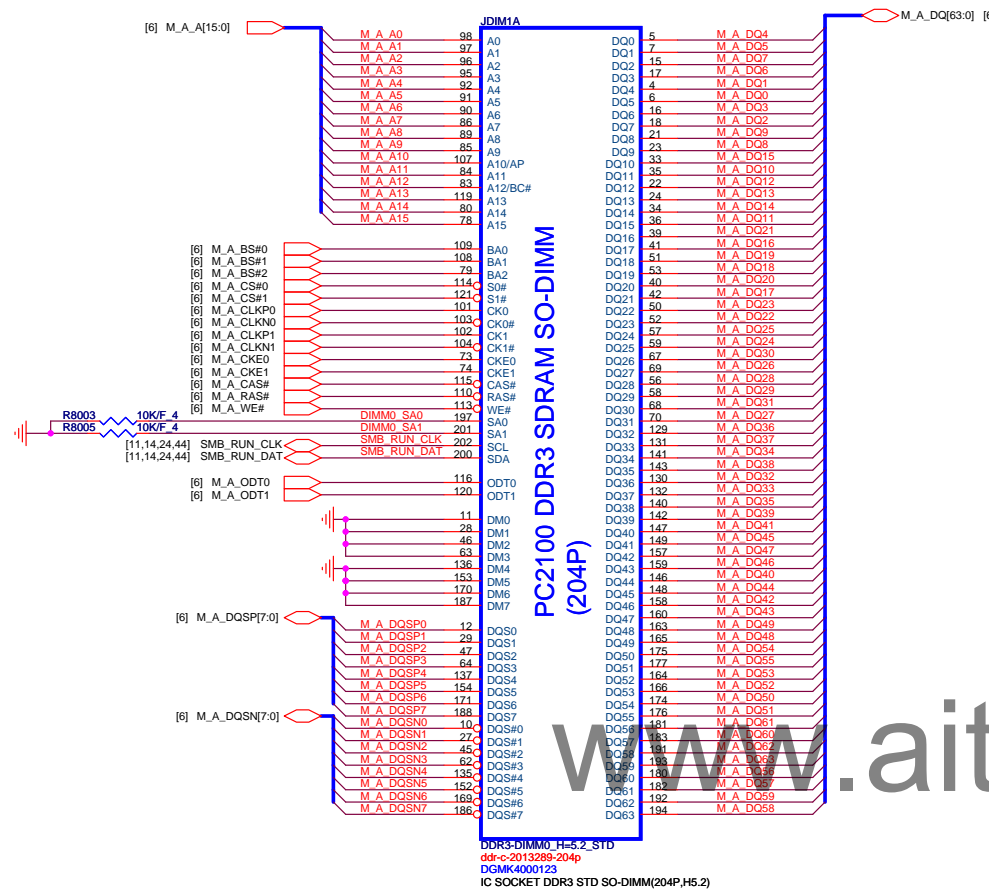


Cougar Point-M (POWER)

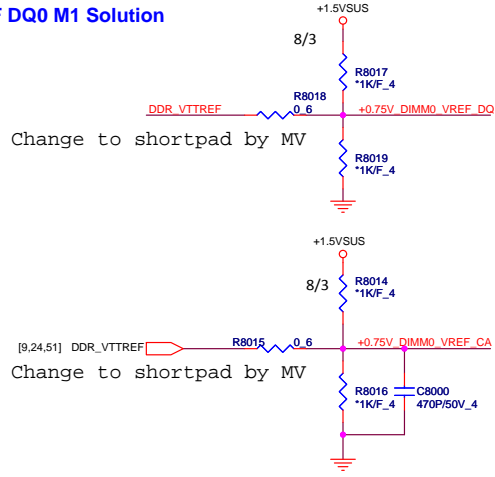




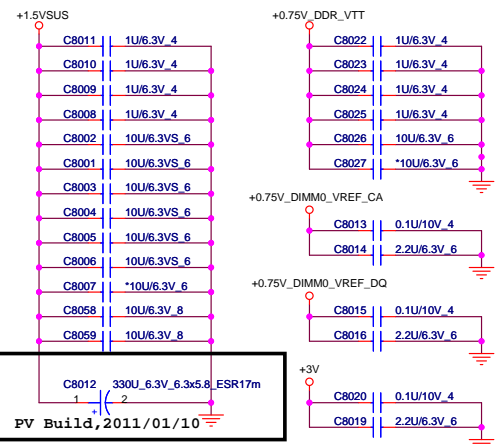




VREF DQ0 M1 Solution

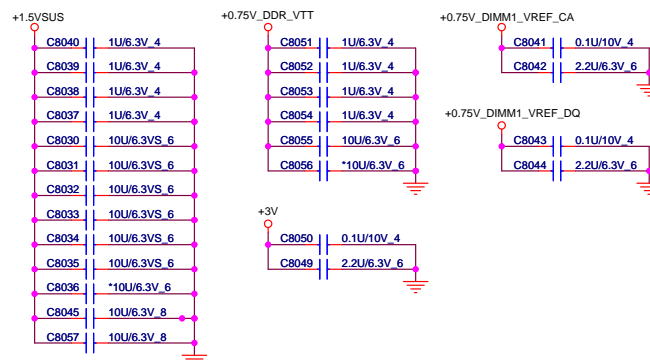


Place these Caps near So-Dimm0.

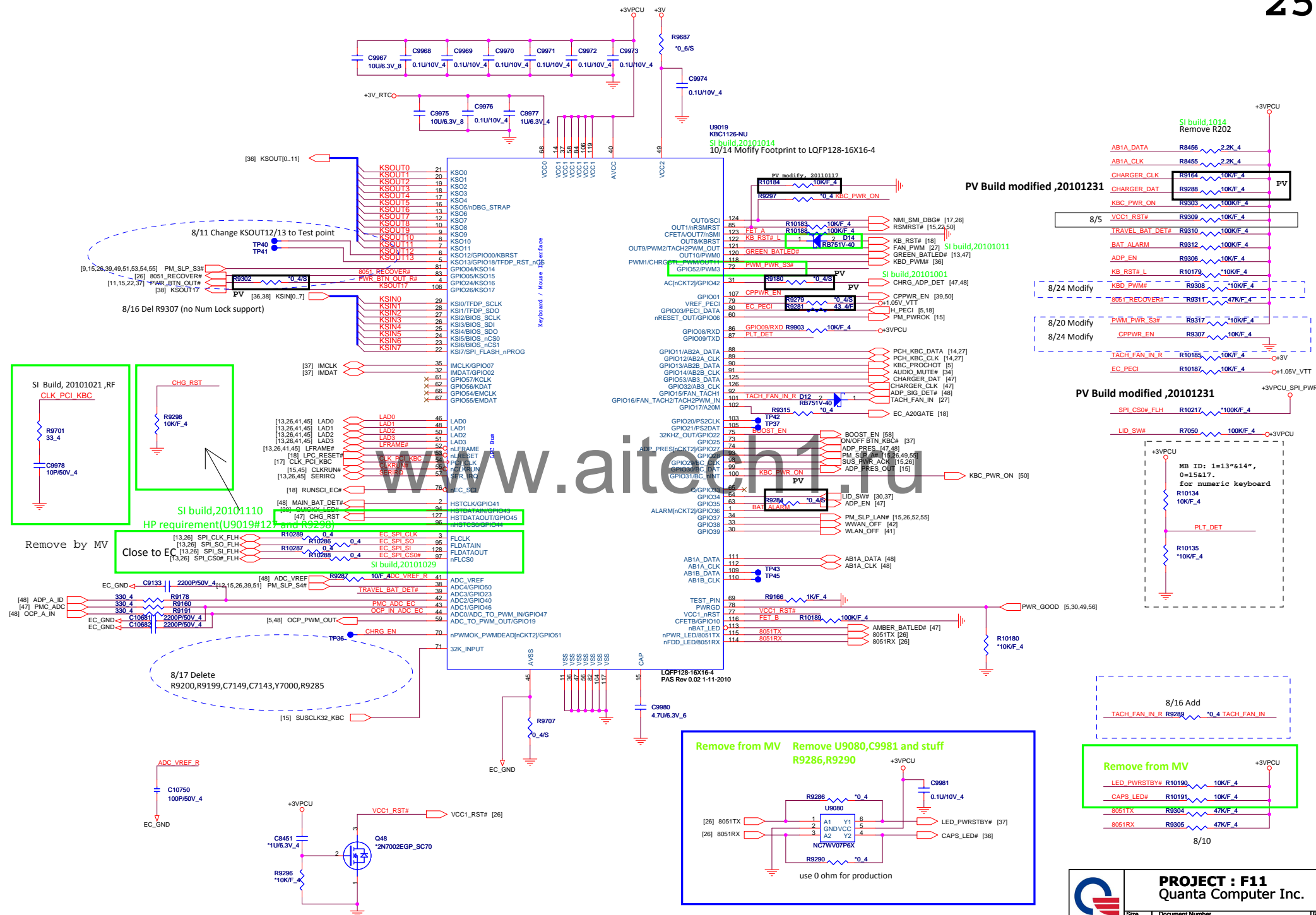




**Place these Caps near So-Dimm1.**

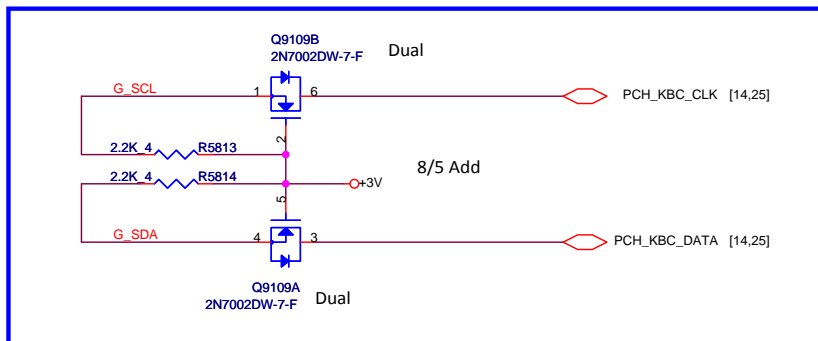
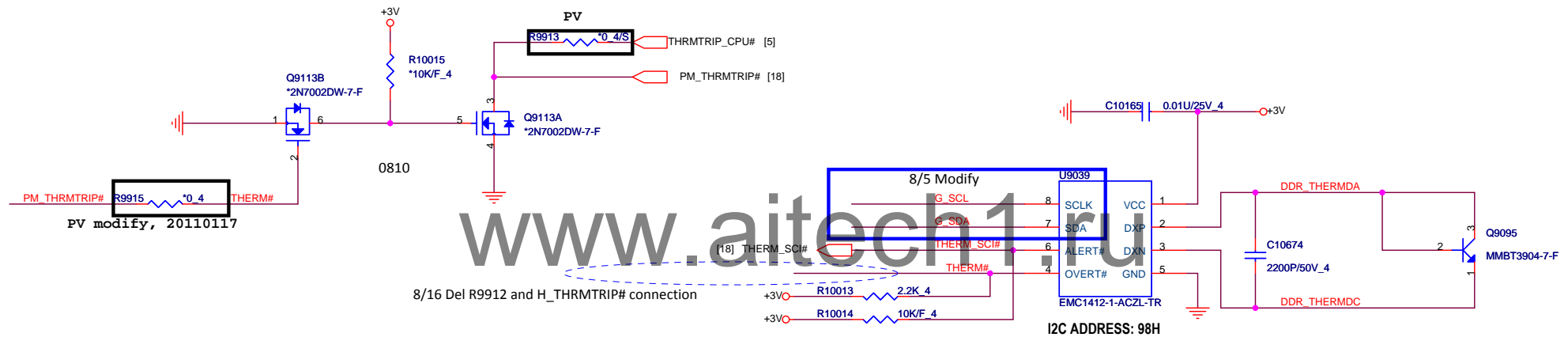
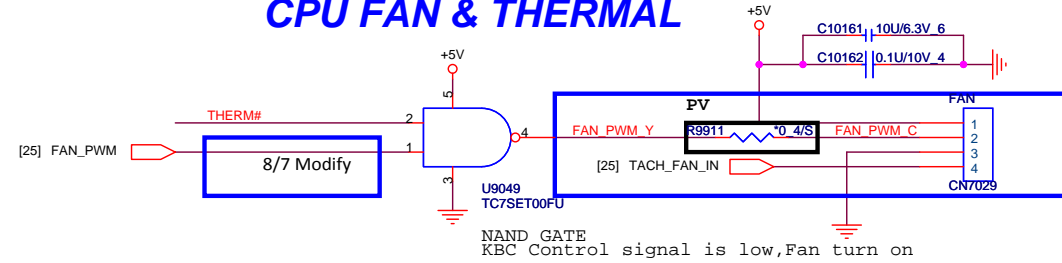


Date: Wednesday, January 19, 2011 Sheet 24 of 58





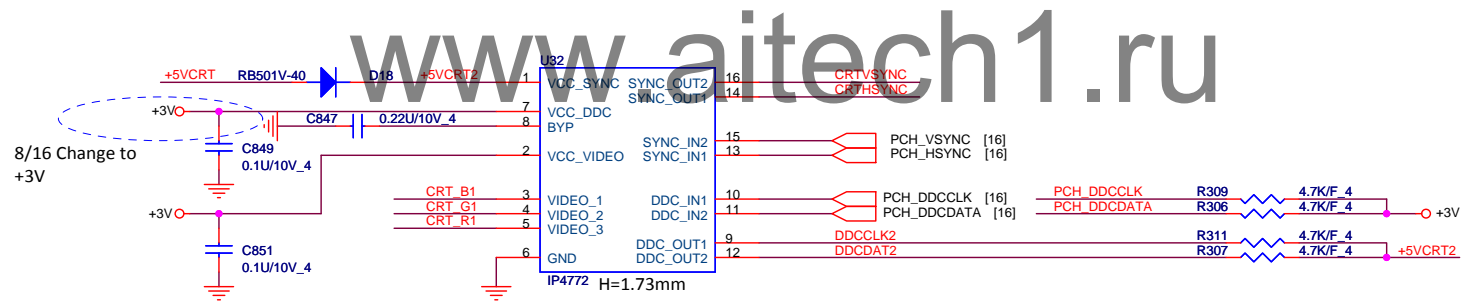
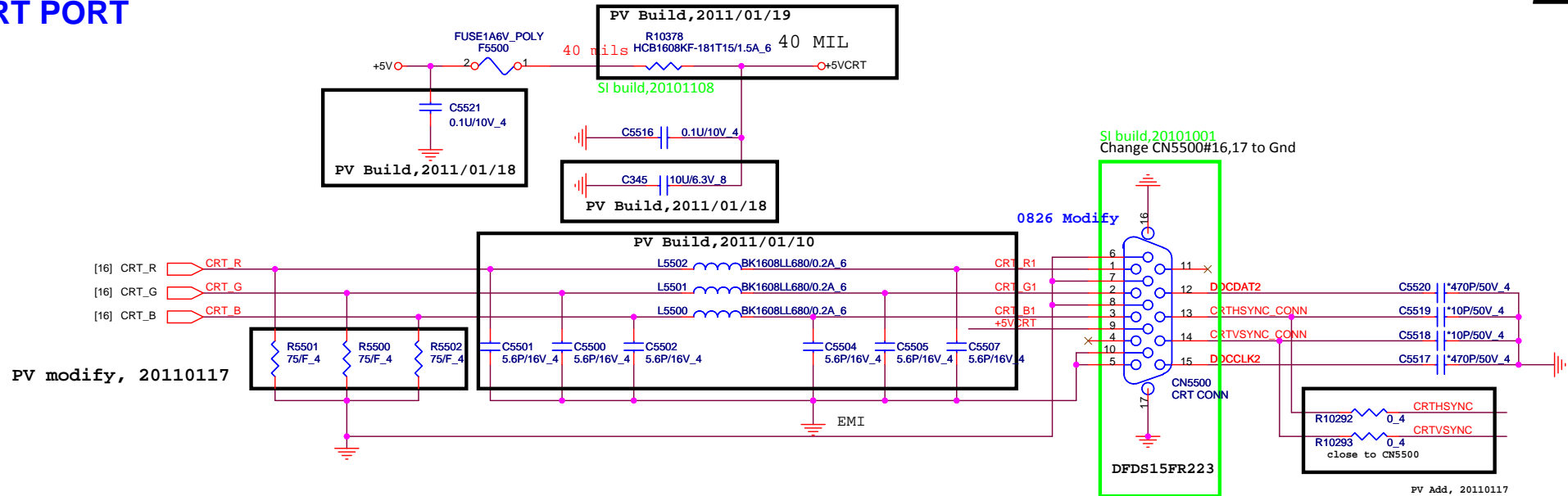
## CPU FAN & THERMAL



**PROJECT : F11**  
Quanta Computer Inc.

Size B	Document Number <b>Thermal / FAN</b>	Rev 1A
Date: Wednesday, January 19, 2011    Sheet 27 of 58		

# CRT PORT



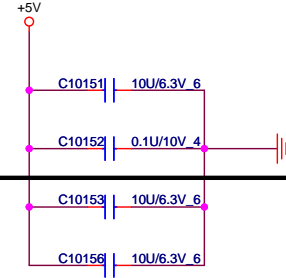
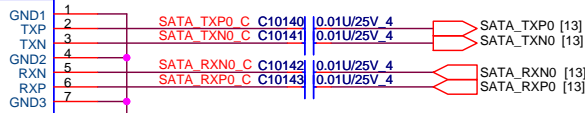
**PROJECT : F11**  
Quanta Computer Inc.

Size B	Document Number <b>CRT</b>	Rev 1A
Date: Wednesday, January 19, 2011 Sheet 28 of 58		

# SATA HDD CONNECTOR

DFHD22MR015

CN7027 LD2722F-SRLL6

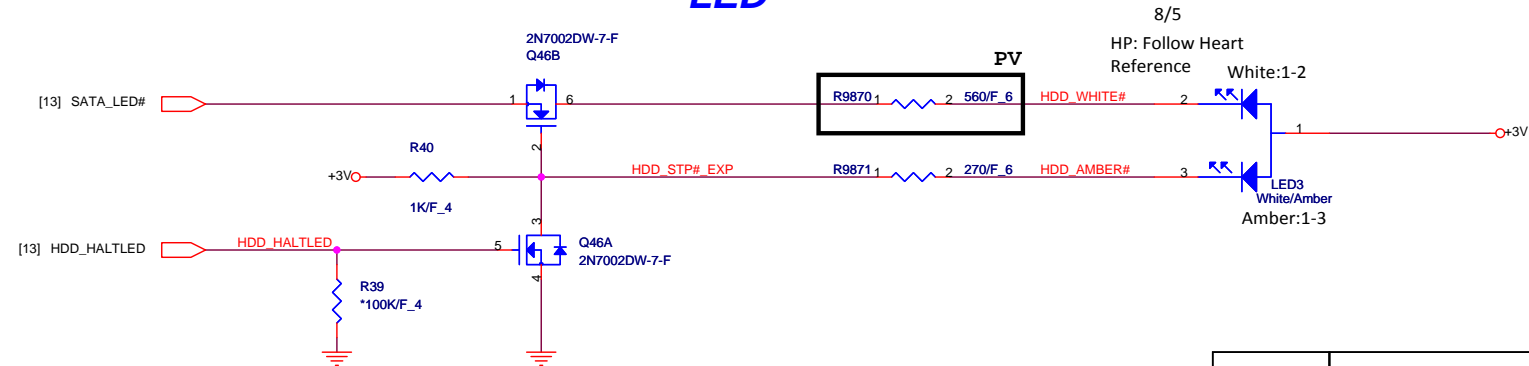


SI build, 20101028  
10/28 Modify CN7027#25, 26 to dummy net

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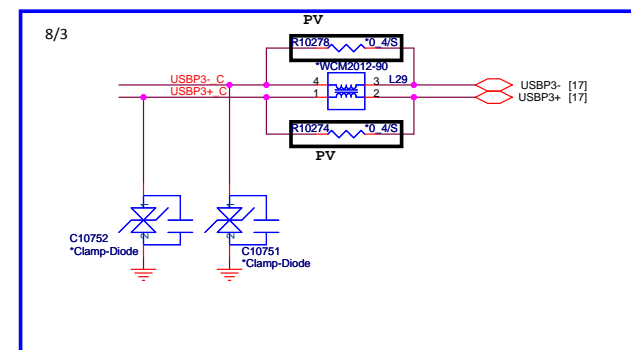
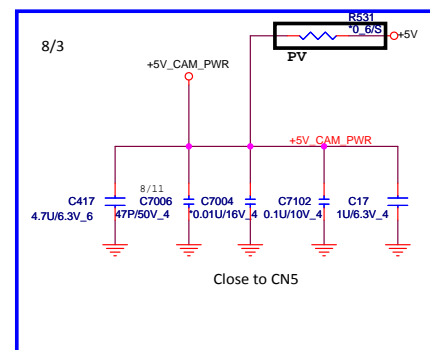
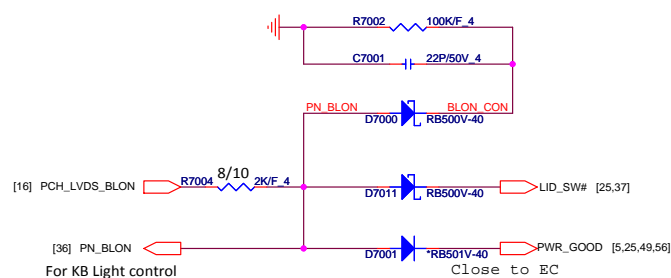
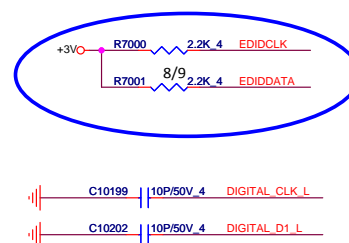
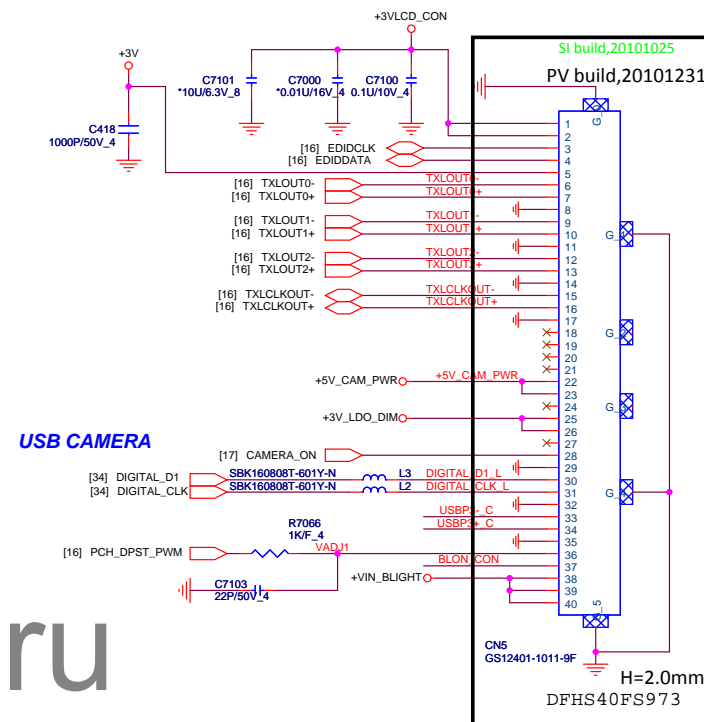
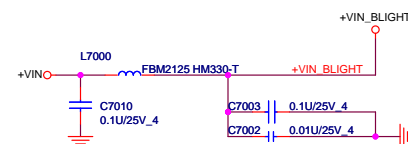
## LED

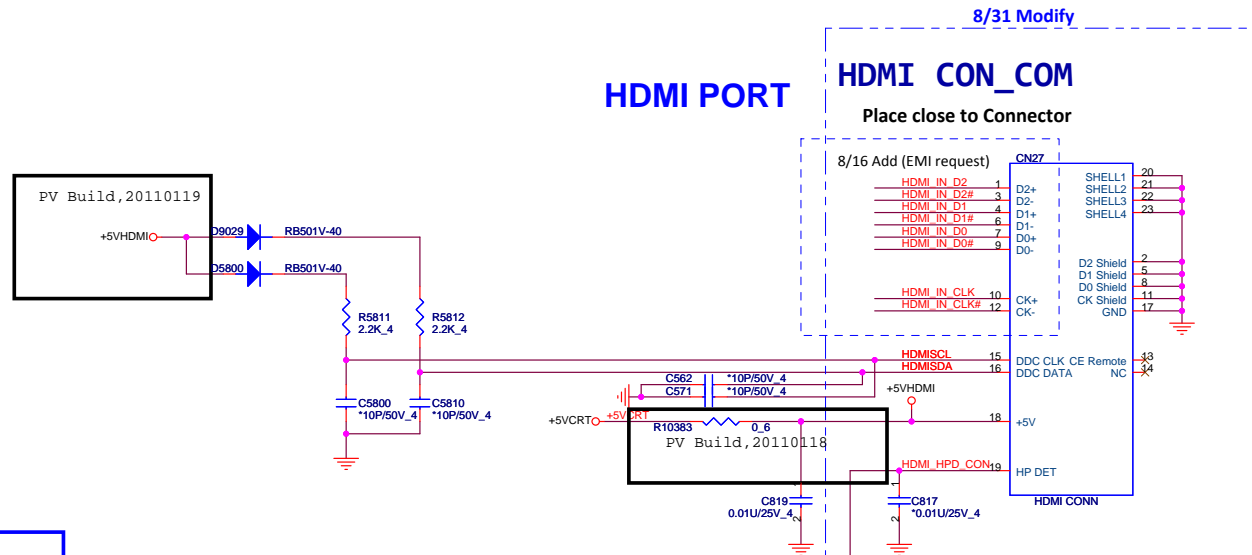
8/10



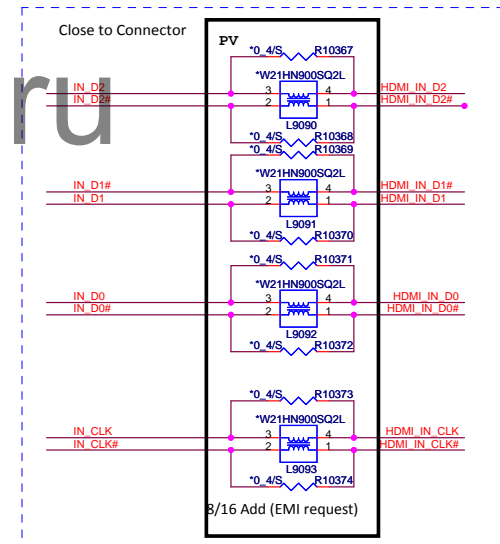
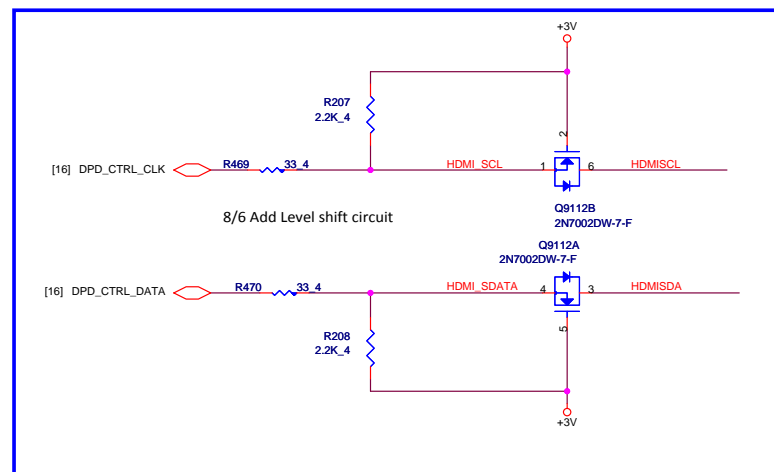
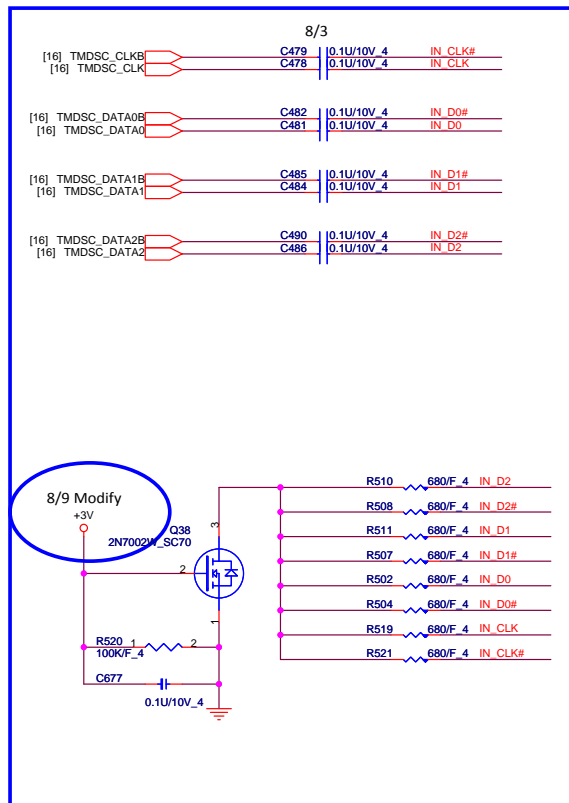
**PROJECT : F11**  
Quanta Computer Inc.

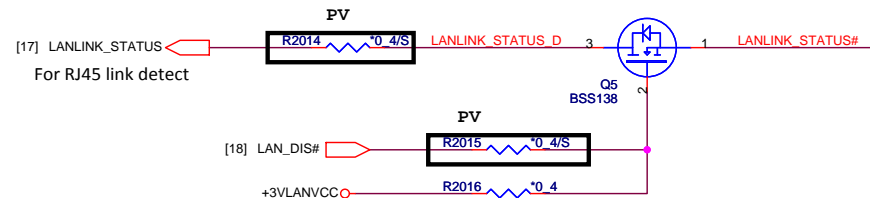
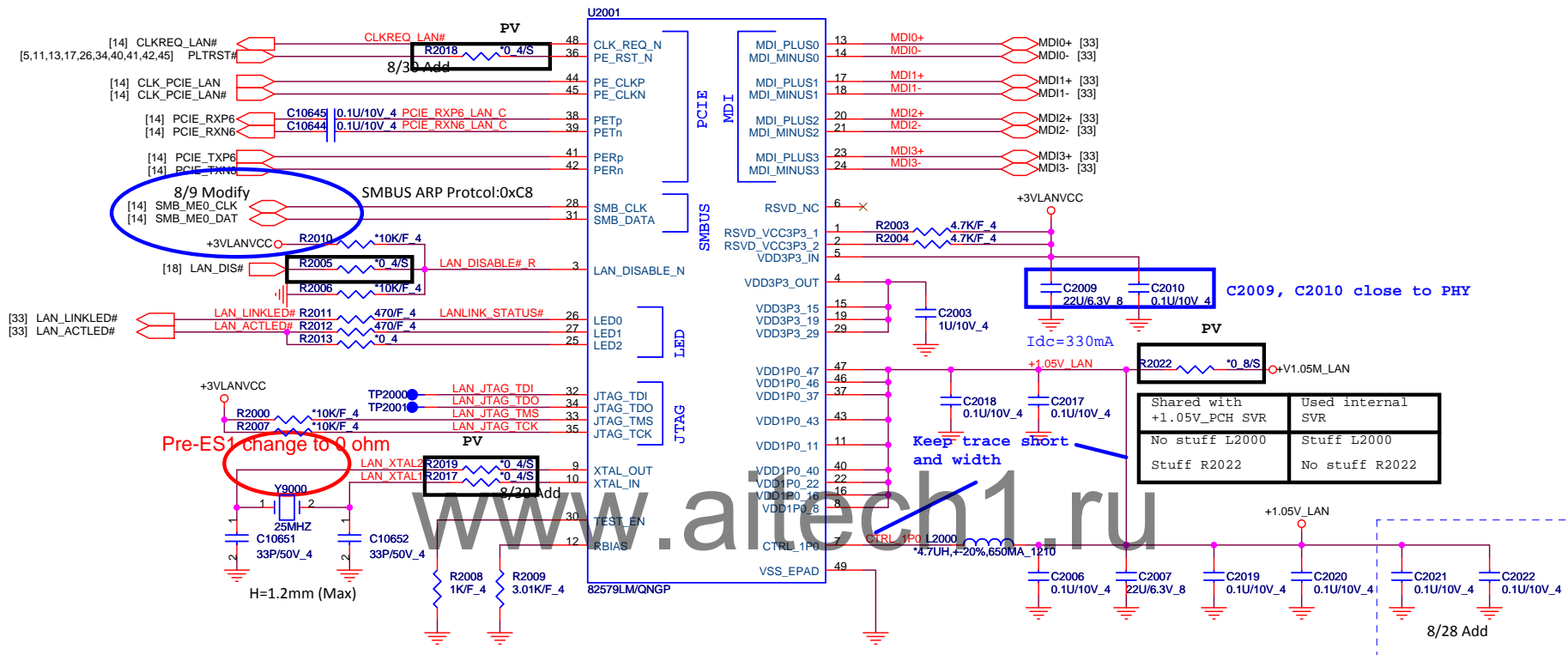
Size B	Document Number	Rev
	<b>HDD/HDD LED</b>	1A
Date: Wednesday, January 19, 2011	Sheet 29 of 58	





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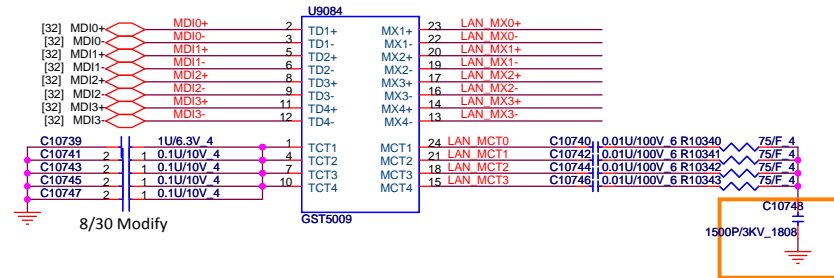




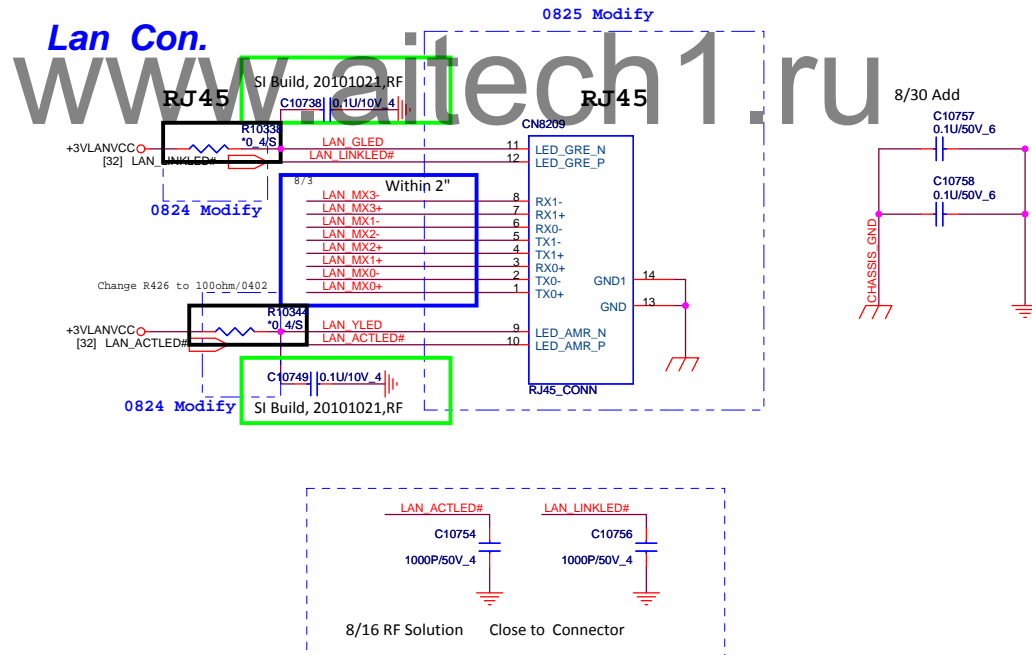
**PROJECT : F11**  
Quanta Computer Inc.

Size B	Document Number	Rev 1A
	Intel Lewisville 82579LM	
Date: Wednesday, January 19, 2011	Sheet 32 of 58	

### Transformer for 10/100/1000

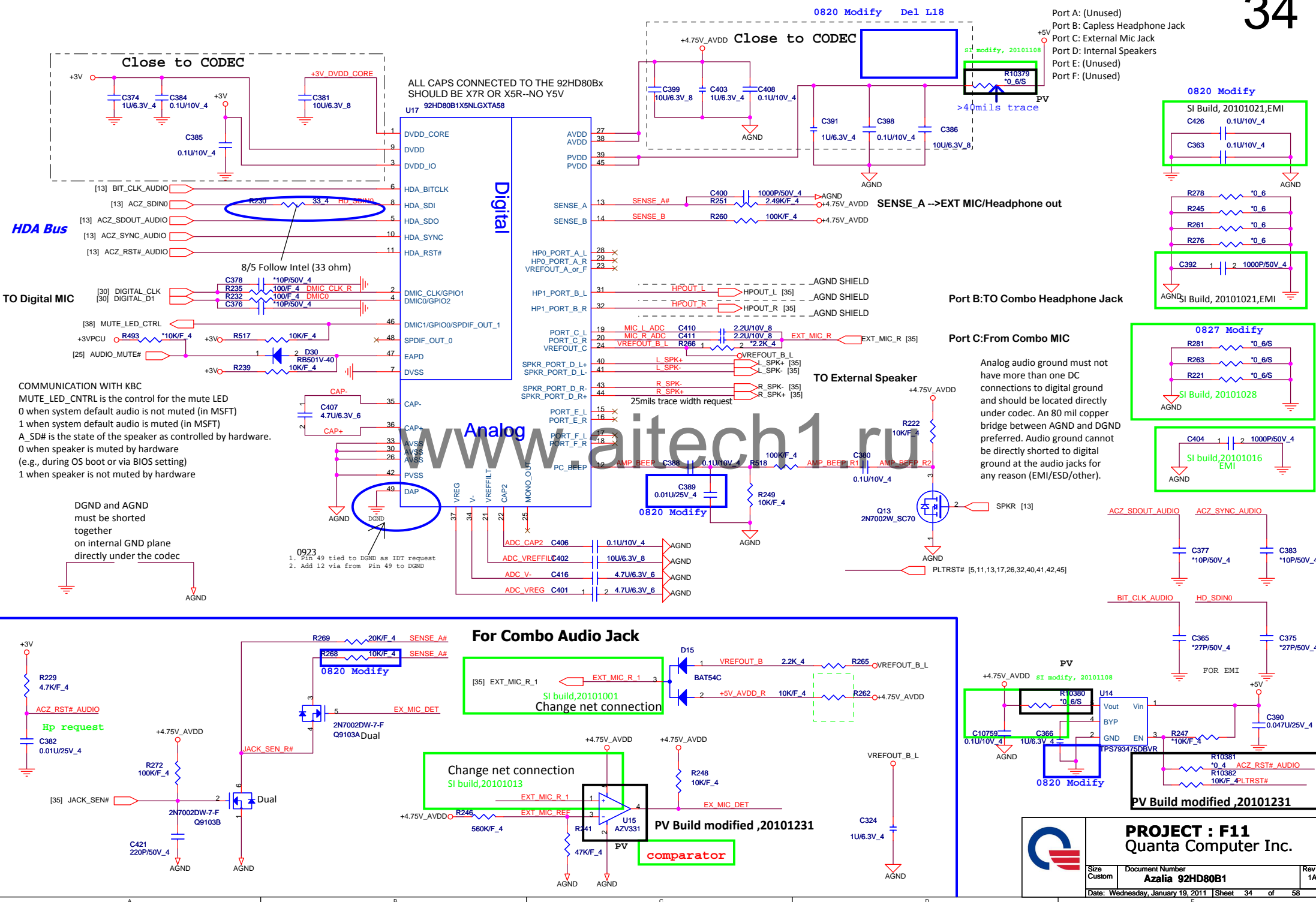


### Lan Con.

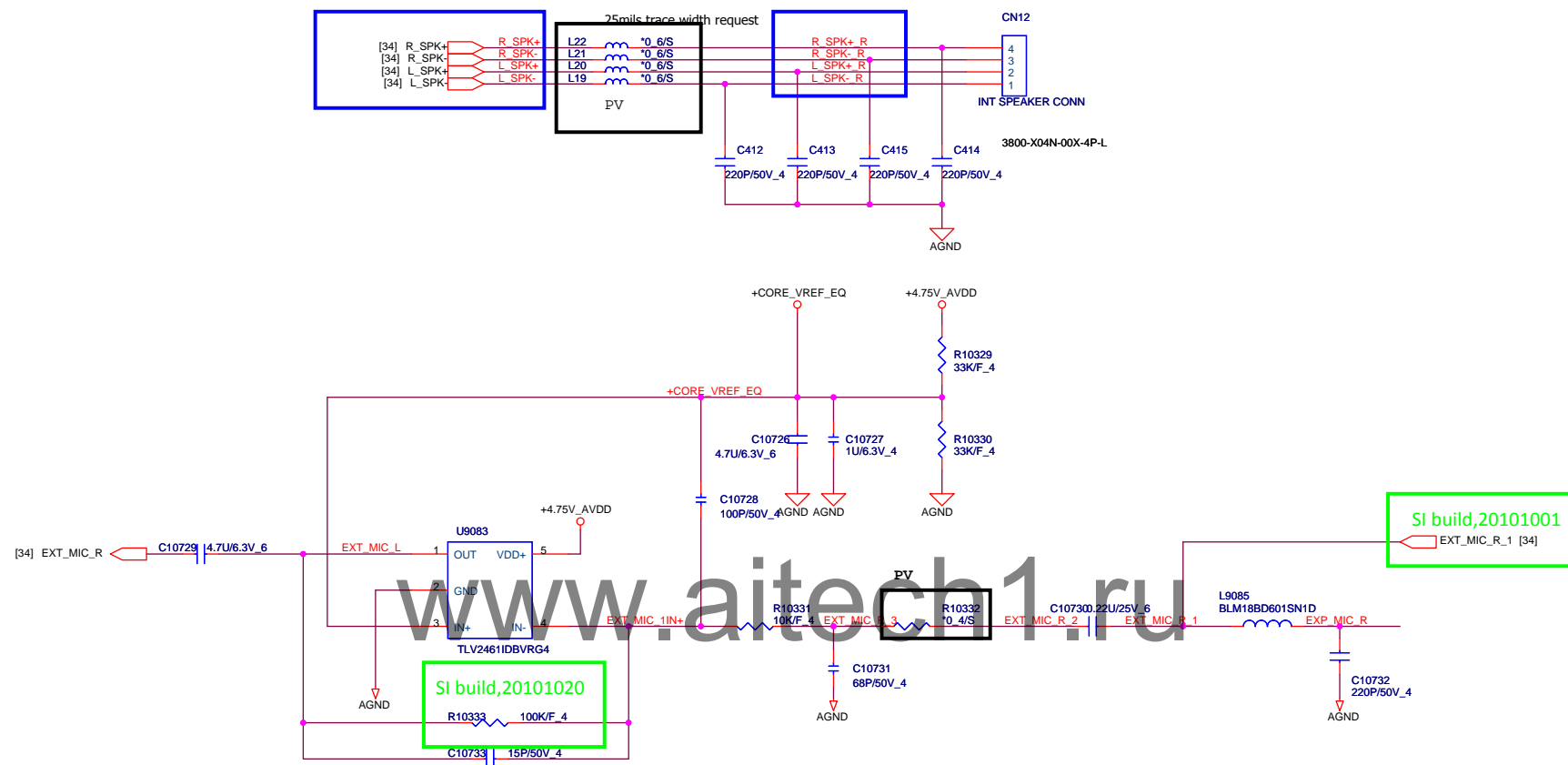


**PROJECT : F11**  
Quanta Computer Inc.

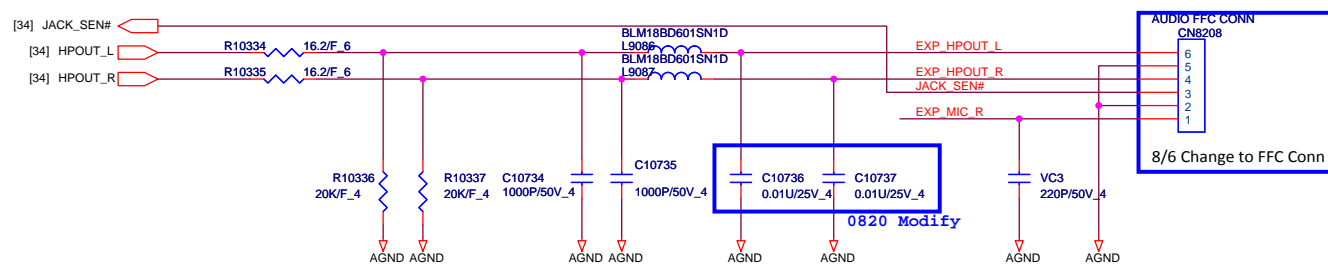
Size Custom	Document Number <b>RJ45 CONN</b>	Rev 1A
Date: Wednesday, January 19, 2011   Sheet 33 of 58		



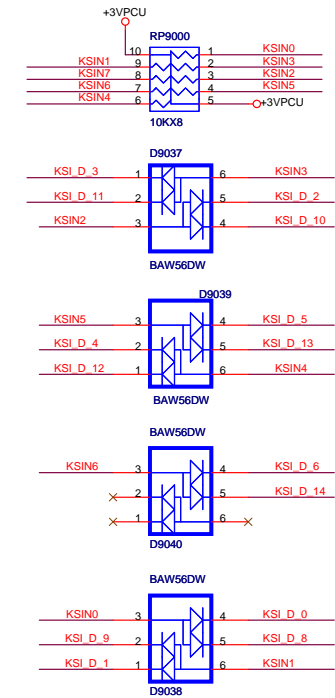
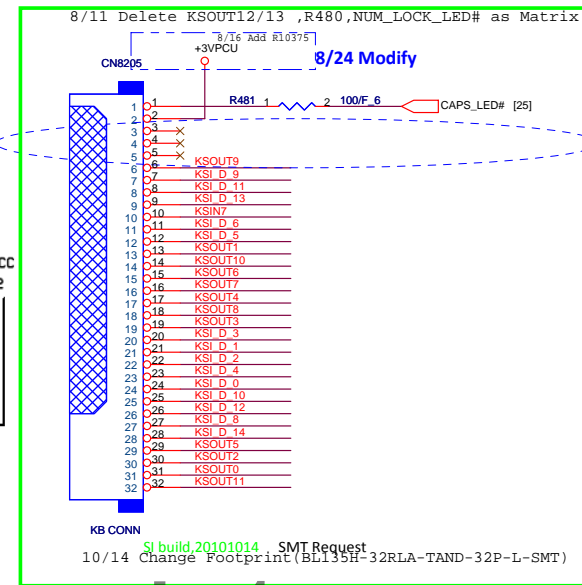
**INT. SPEAKER**



### ***Combo Jack (Headphone/MIC)***



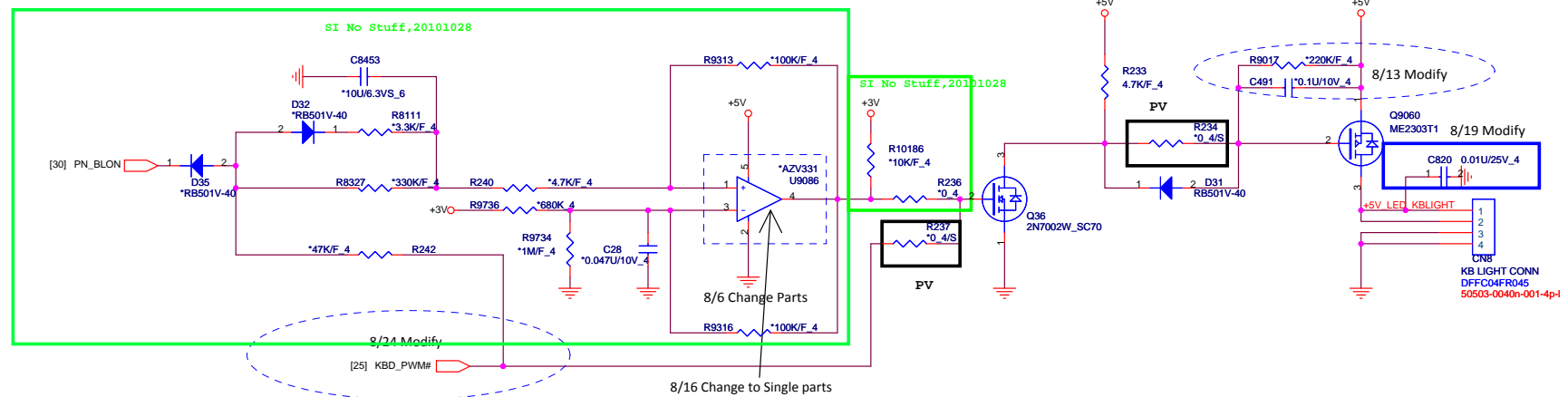
[25] KSOUT[0..11]  $\rightarrow$  KSOUT0..11  
 [25..38] KSIN[0..7]  $\rightarrow$  KSIN0..7



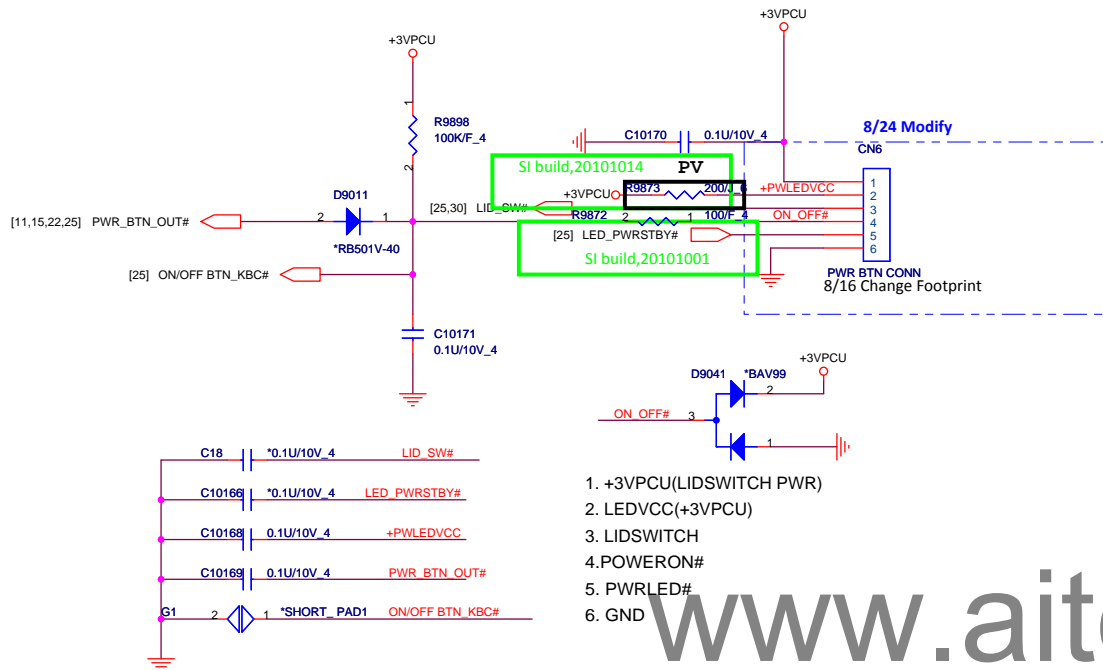
KSI_JN(0)	24	46	47	48	133	42	21	22	53	54	29	43	
KSI_JN(1)	21	17	18	19	125	26	20	23	24	25	76	129	
KSI_JN(2)	22	31	32	33	117	40	5	8	38	39	13	27	
KSI_JN(3)	20	2	3	4	80	11	34	37	9	10	120	121	
KSI_JN(4)	23	1	30	110	75	12	50	51	81	14	89	123	
KSI_JN(5)	12	114		112	84	28	35	36	86	127	79	15	
KSI_JN(6)	11	113	115	16	61	119	49	52	118	56	85	122	
KSI_JN(7)	10	45		116	131	55	6	7	41	126	132	83	
KSI_JN(8)	27											44	
KSI_JN(9)	7											57	
KSI_JN(10)	25											60	
KSI_JN(11)	8											62	
KSI_JN(12)	26											59	
KSI_JN(13)	9											64	
KSI_JN(14)	28											58	
		31	13	30	19	17	29	15	16	18	6	14	32
		(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)

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KEYBOARD LIGHT CONTROL

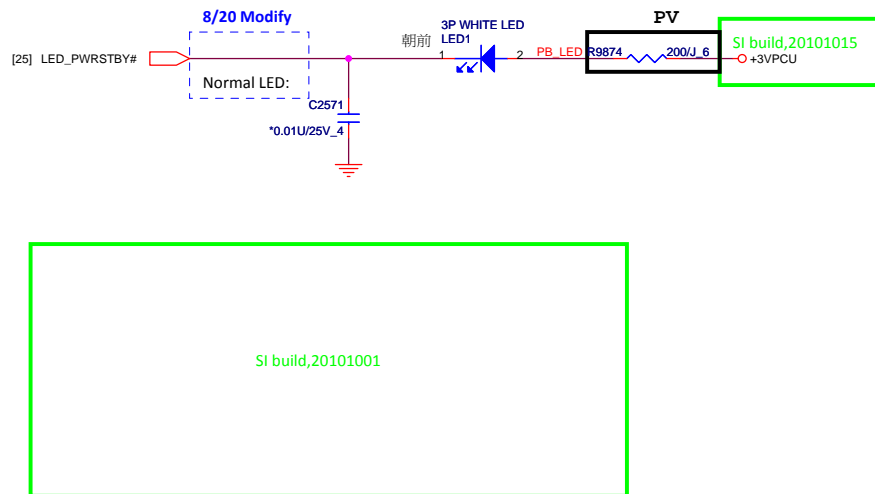


## POWER BOTTON CONNECT

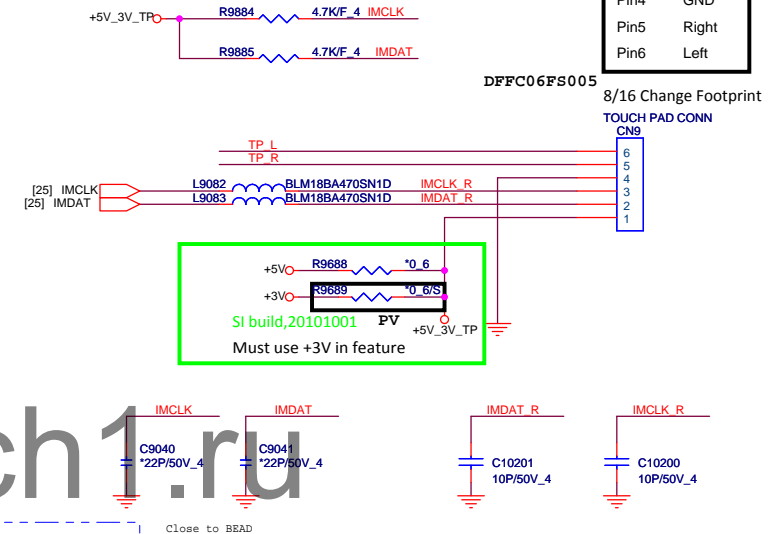


09/01 Modify

## PWR LED

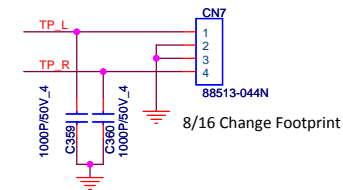


## TOUCH PAD CONNECTOR



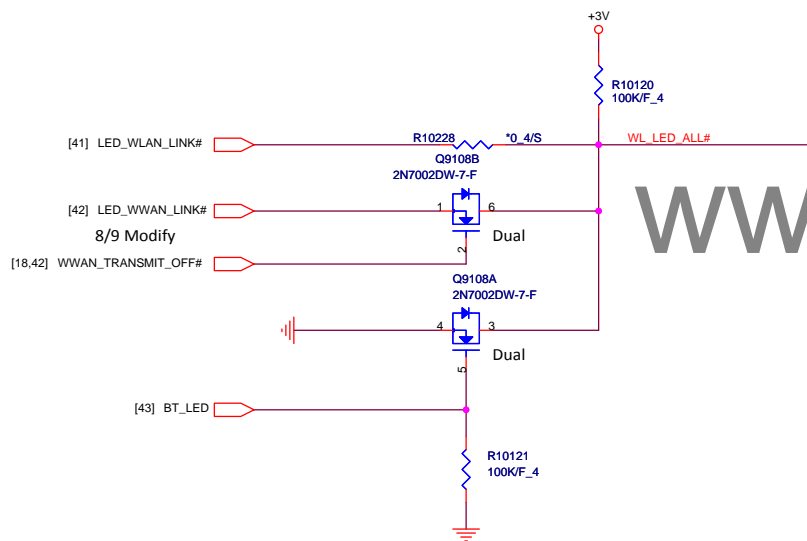
Close to BEAD

## TOUCH PAD SW CONN



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Quanta Computer Inc.

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**Touch Pad,TP SW,PWR CONN** Rev 1A  
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## Function Board(Mute/Quickweb/Wireless)

### KSIO (MUTE)

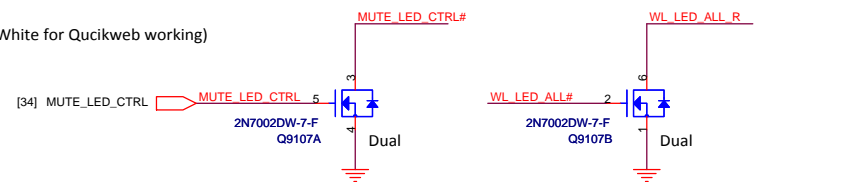
Mute LED: Amber when  
Mute(Single Color)

### KS11 (WIRELESS)

Dual Color (White/Amber)  
Wireless LED: Wireless ON(White) and Wireless OFF(Amber)

### KS13 (QUICKX)

Quickweb LED: (White for Quicikweb working)

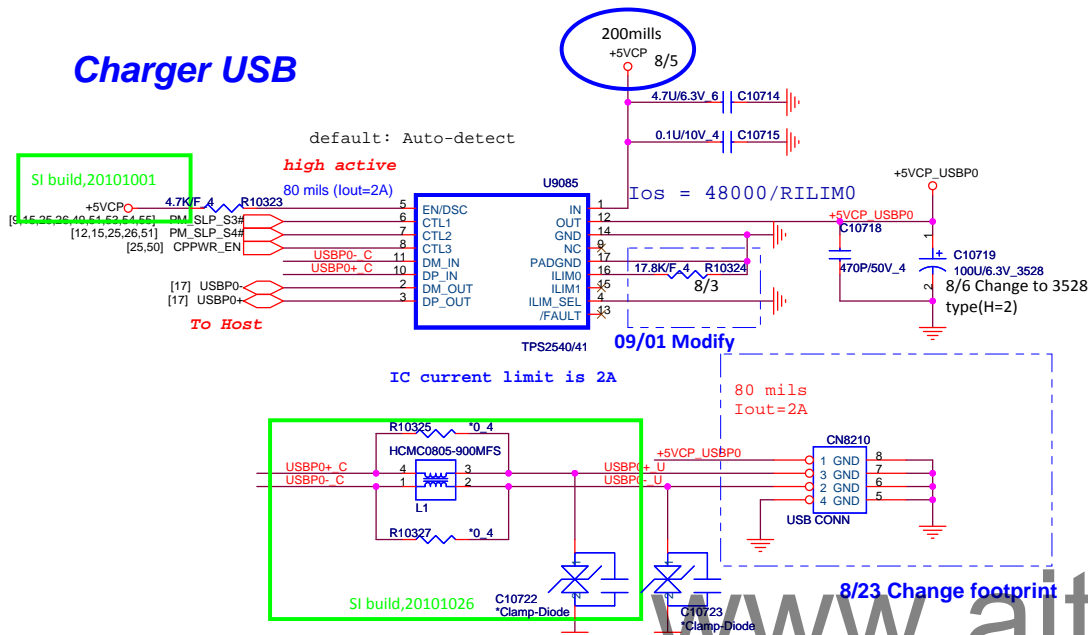


**PROJECT : F11**  
**Quanta Computer Inc.**

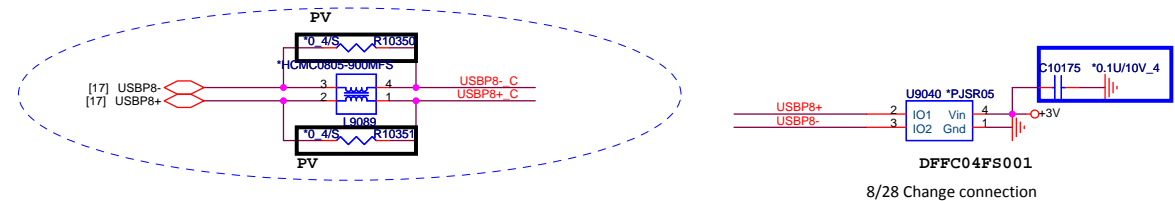
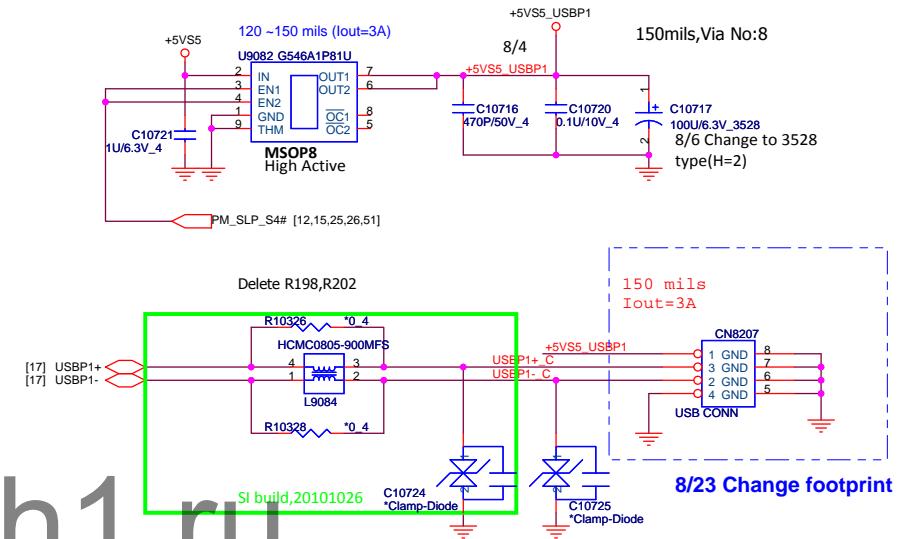
Size Custom	Document Number <b>FUNCTION BOARD</b>	Rev 1A
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**Right SIDE USBX2(Powered USB and Charger USB)**

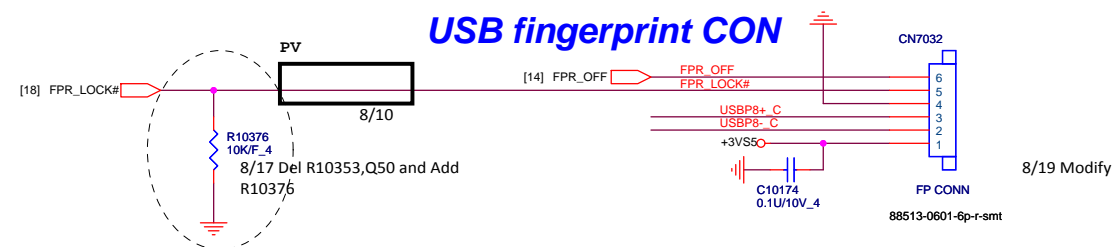
## Charger USB



## Powered USB

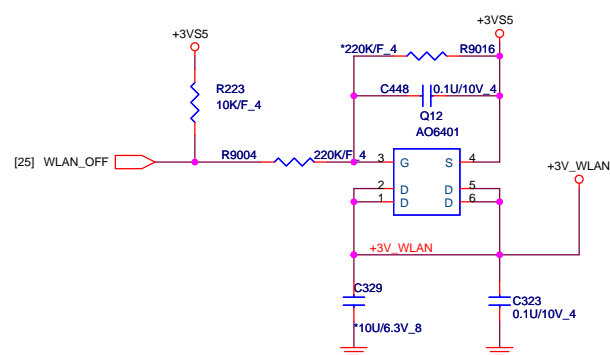
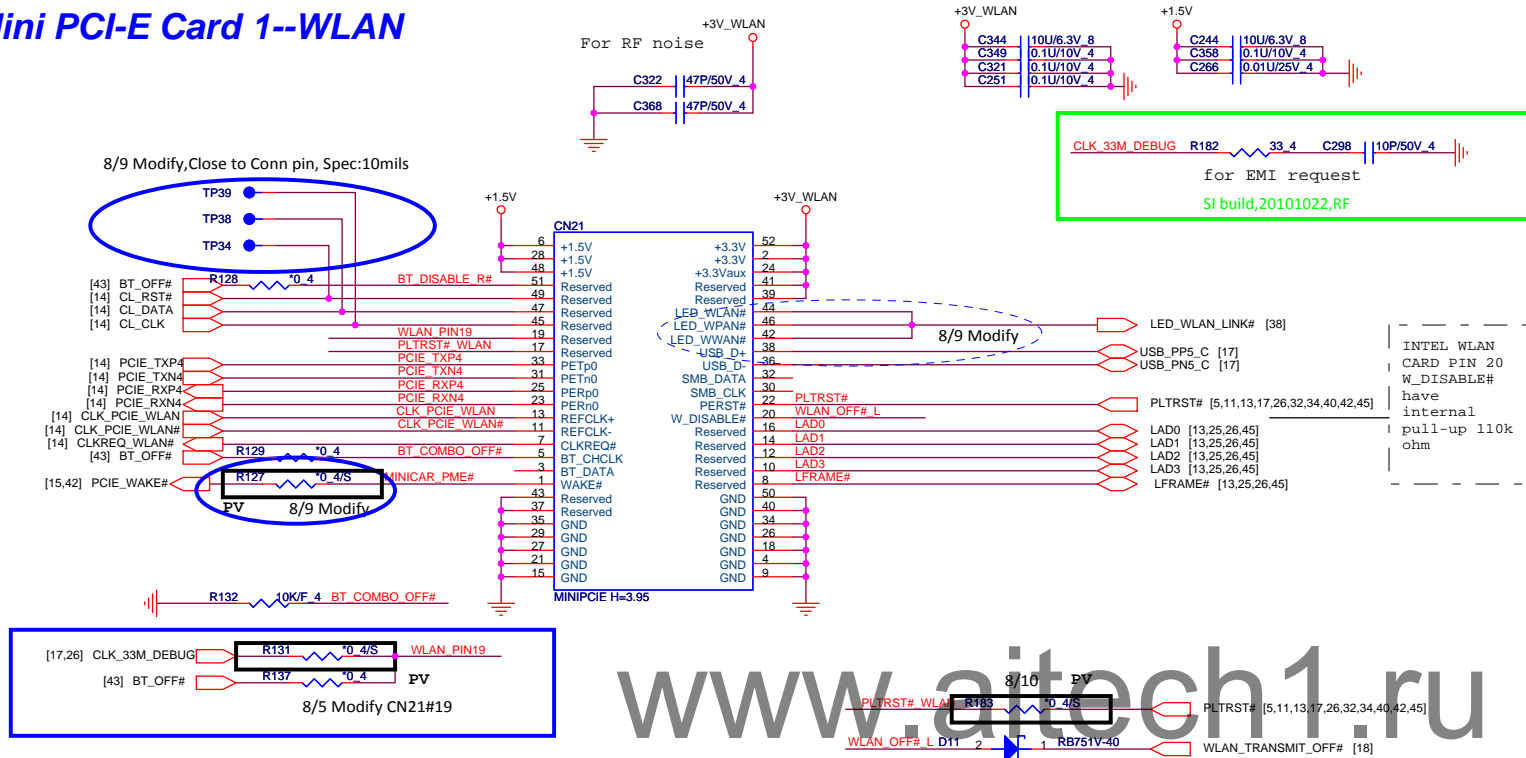


CTL1	CTL2	CTL3	TPS2540 Control Truth Table
0	0	0	Out Discharge ,Power switch OFF
0	X	1	Dedicated Charging Port,Auto
X	1	0	Standard Downstream Port ,USB 2.0
1	0	0	Dedicated Charging Port, BC Specification 1.1
1	0	1	Dedicated Charging Port, Apply
1	1	1	Only Downstream Port, BC Specification 1.1

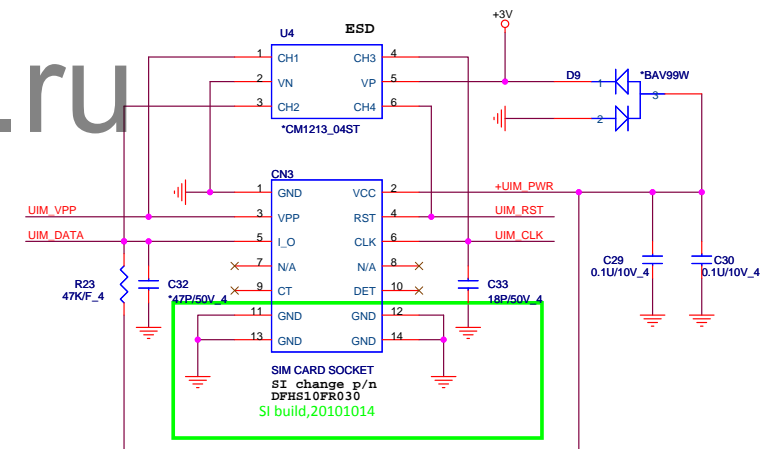
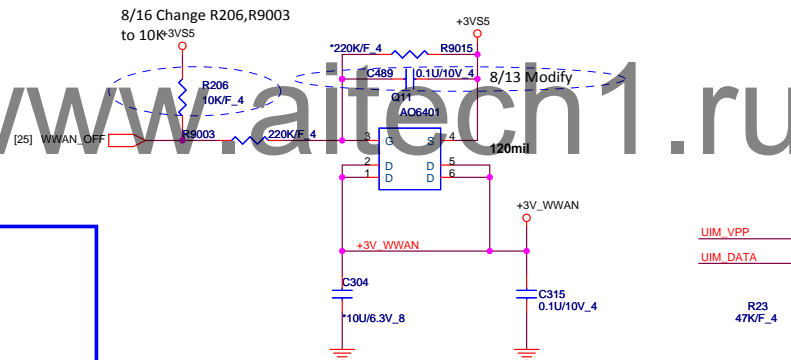
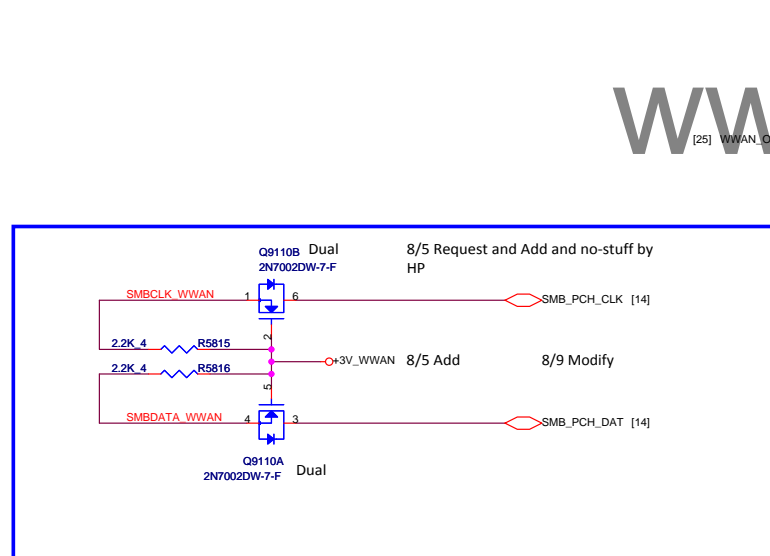
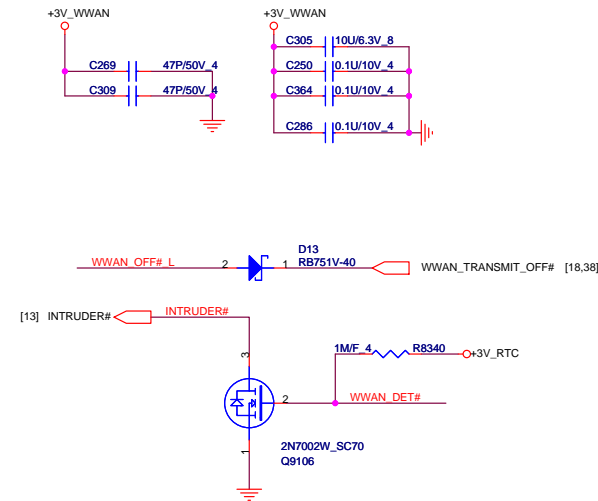
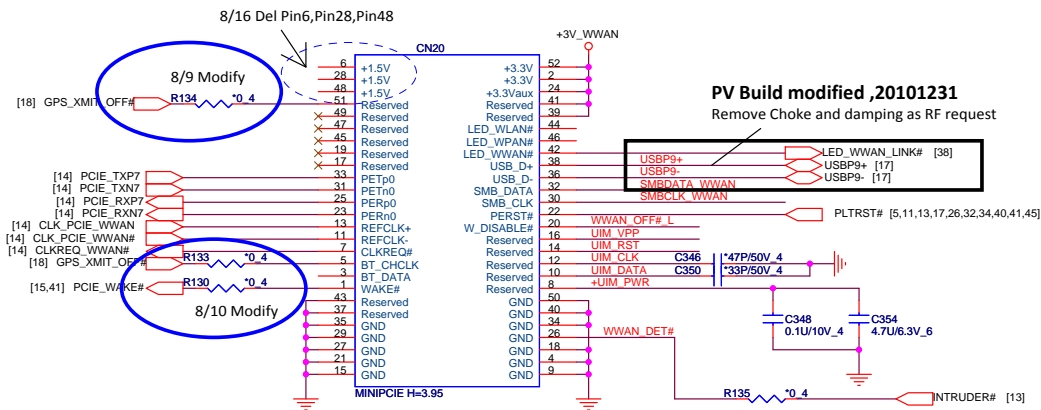




### Mini PCI-E Card 1--WLAN



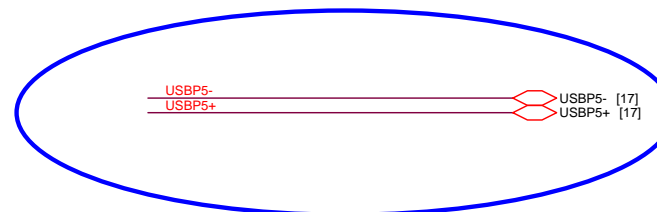
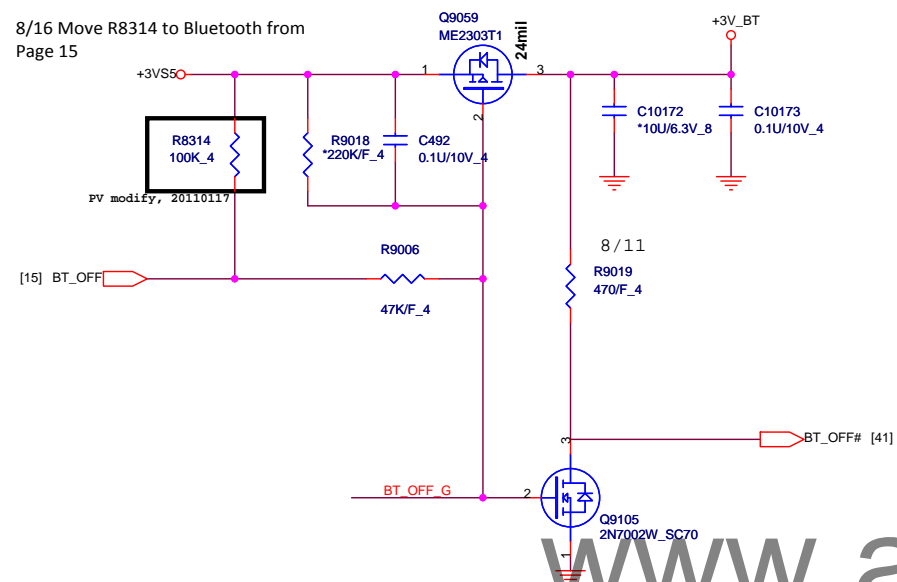
## Mini PCI-E Card 2 --WWAN



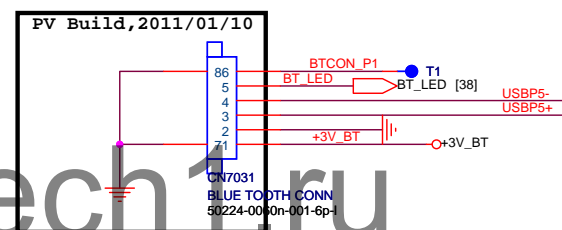
[5,9,12,19,41,49,55] +1.5V  
[11,12,13,14,15,16,17,18,19,20,23,24,25,27,28,29,30,31,34,36,37,38,39,40,44,45,48,49,51,55,56] +3V

# BLUETOOTH

8/16 Move R8314 to Bluetooth from  
Page 15



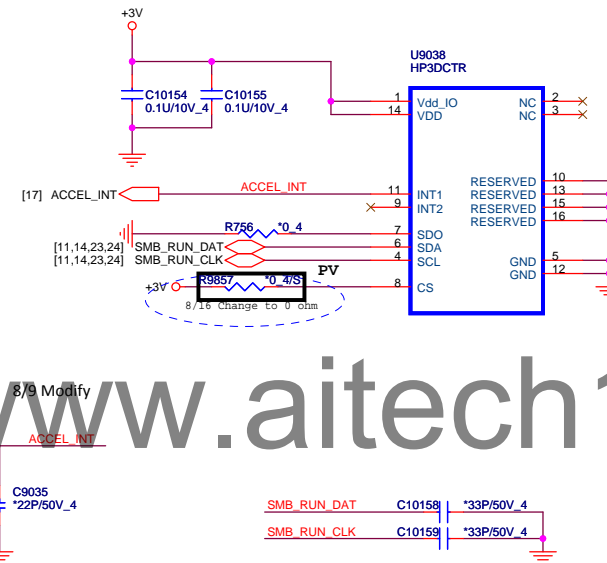
Remove L9081,R10347,R10346 by PV Build  
PV Build,2011/01/18



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## Accelerometer Sensor

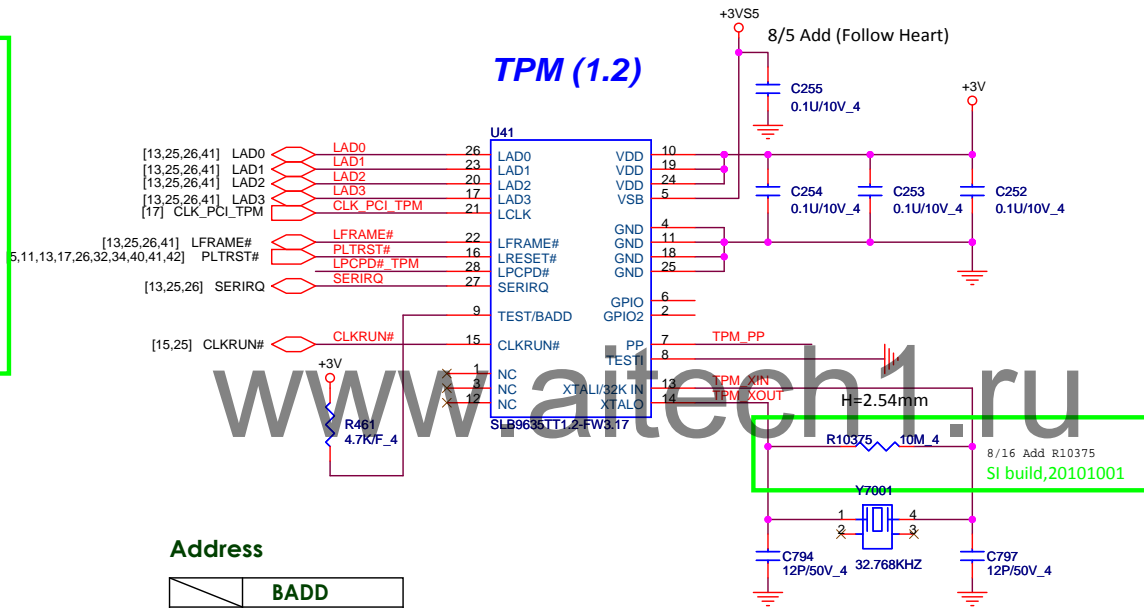
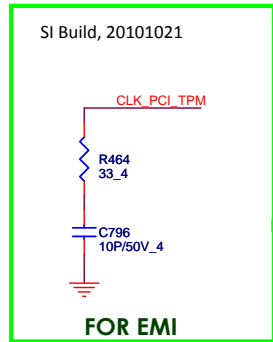


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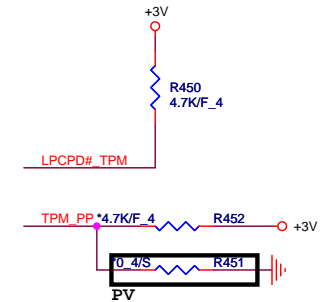
**PROJECT : F11**  
Quanta Computer Inc.

Size Custom	Document Number <b>Accelerometer Sensor</b>	Rev 1A
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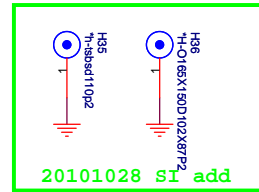
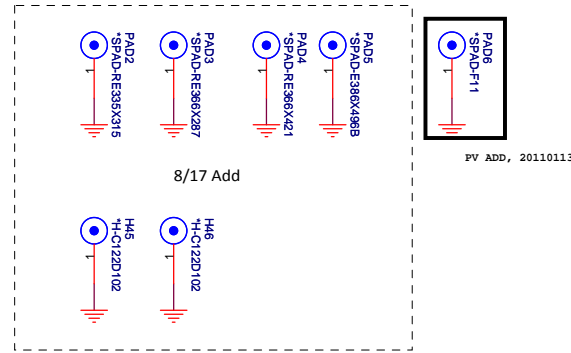
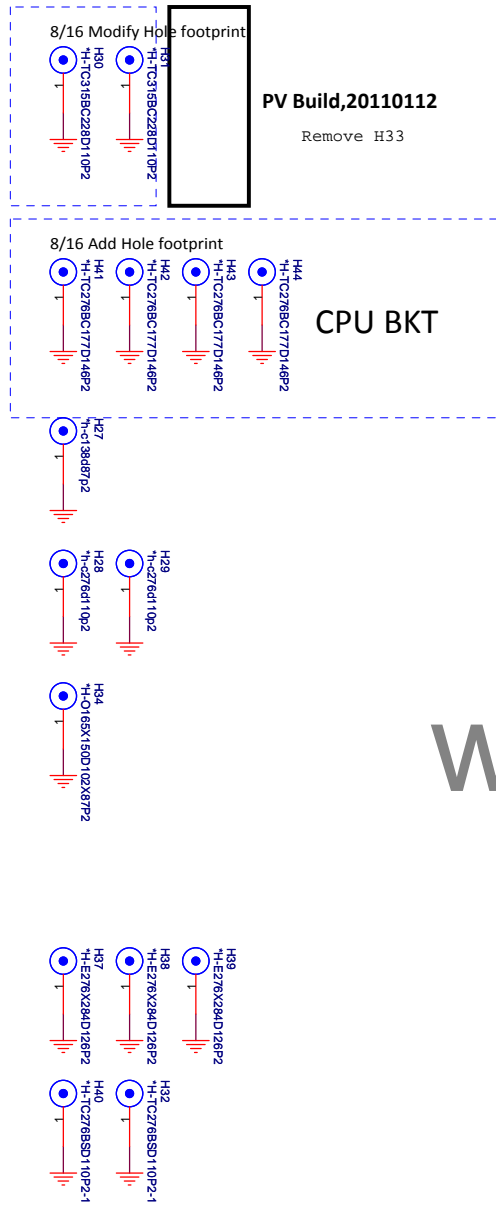


**Address**

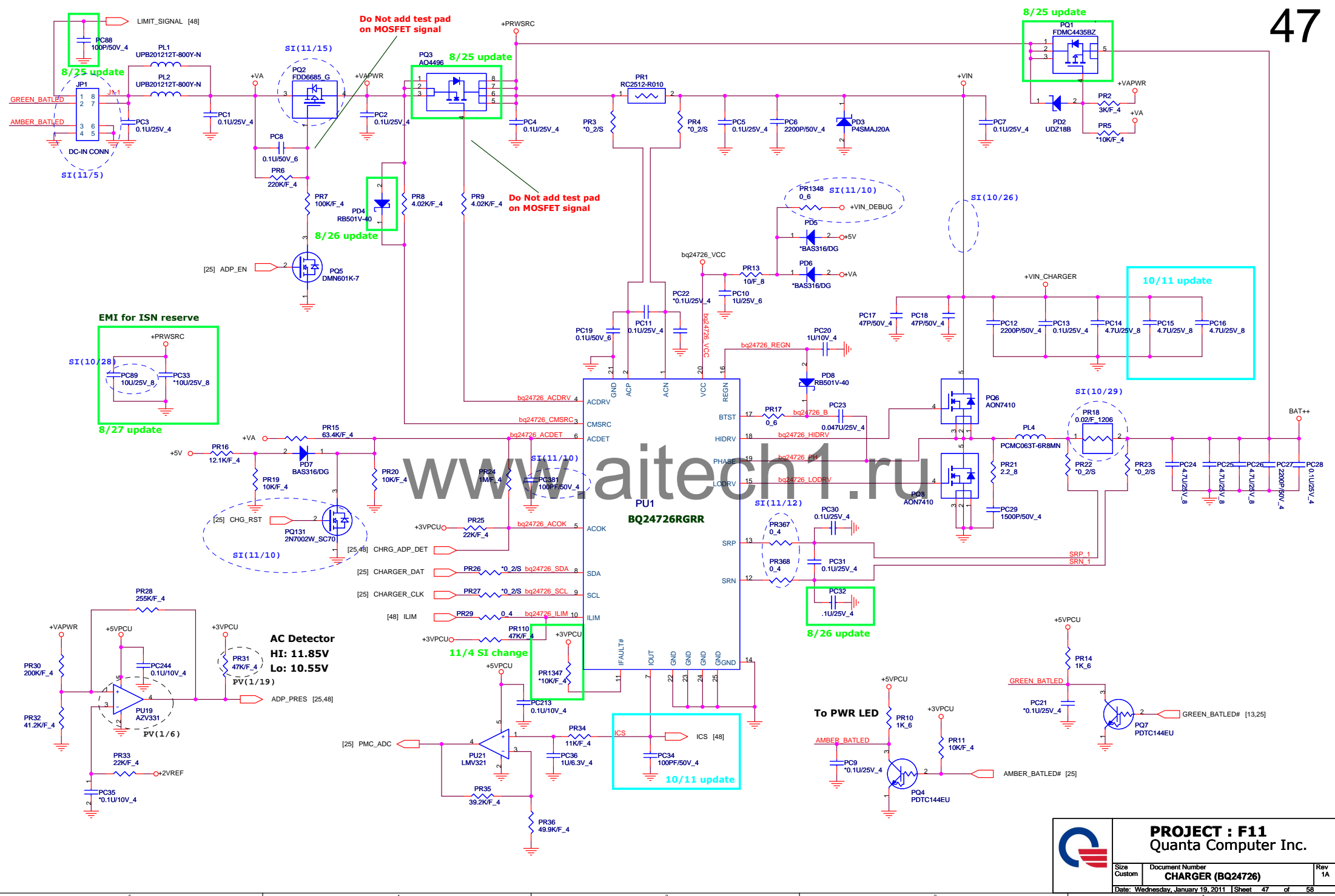
	BADD
HIGH	4EH/4F (default)



<p><b>PROJECT : F11</b> Quanta Computer Inc.</p>		
Size B	Document Number <b>TPM</b>	Rev 1A
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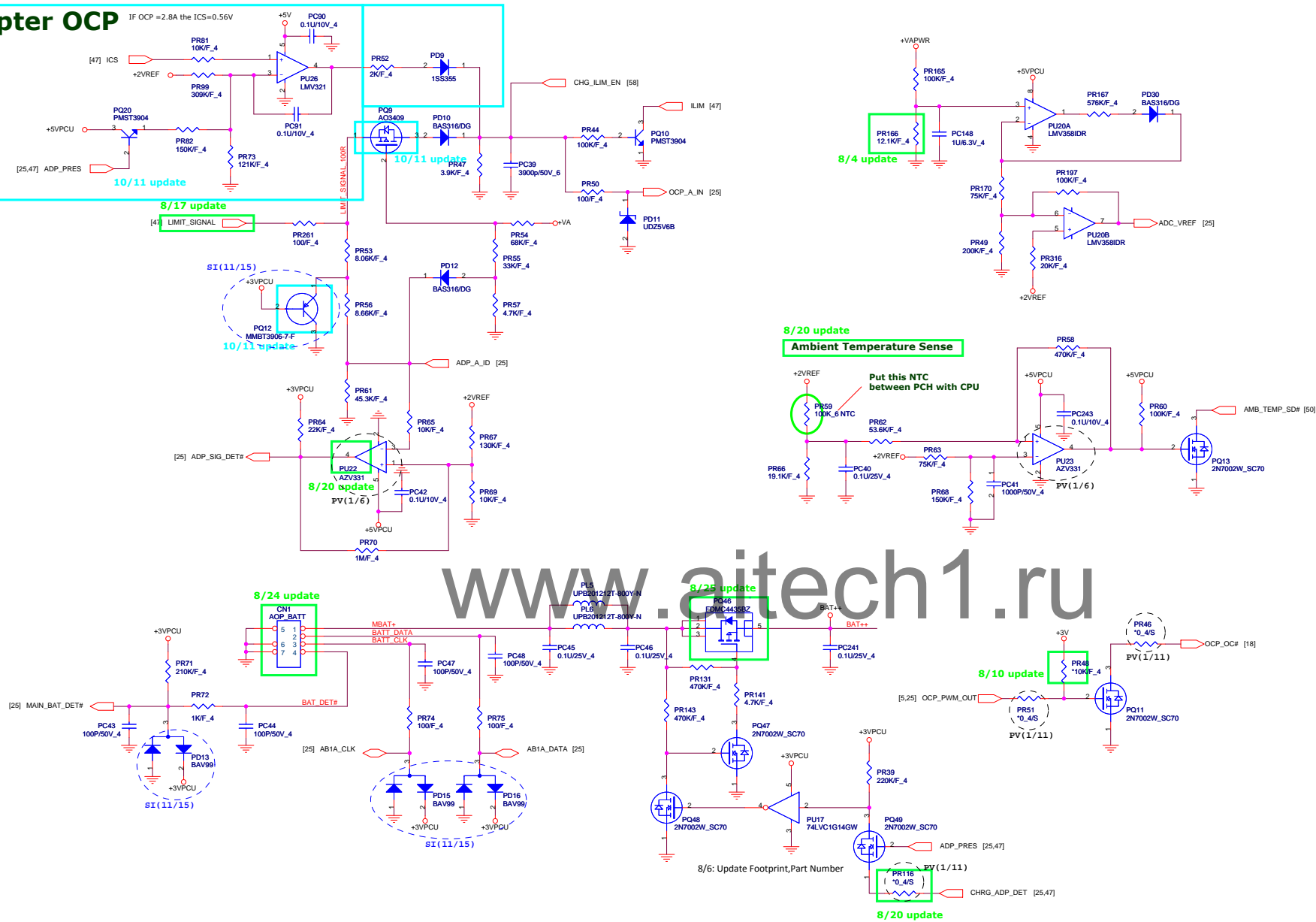


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## Adapter OCP

IF OCP = 2.8A the ICS=0.56V



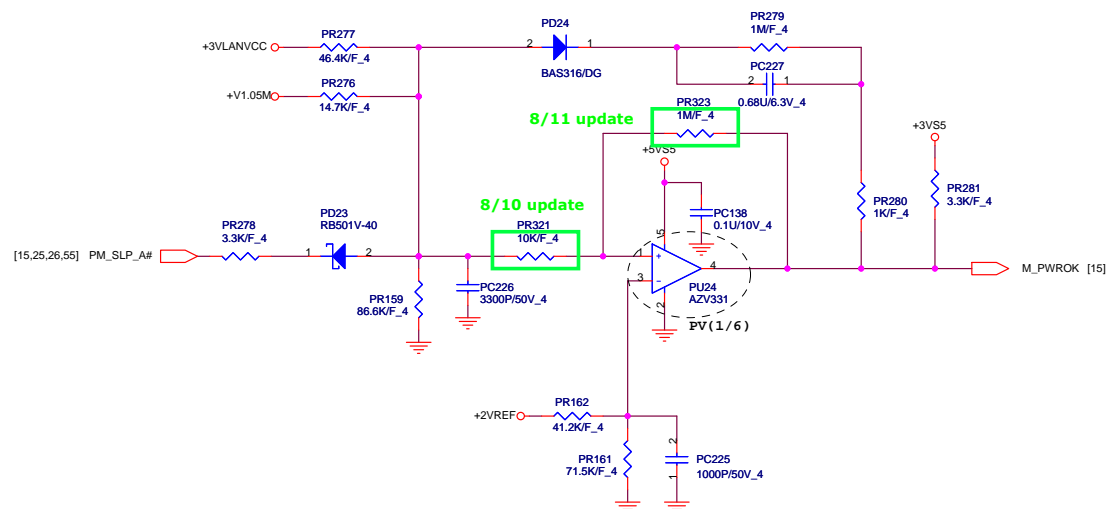
**PROJECT : F11**  
**Quanta Computer Inc.**

Size C	Document Number <b>CHARGERII</b>	Rev 1A
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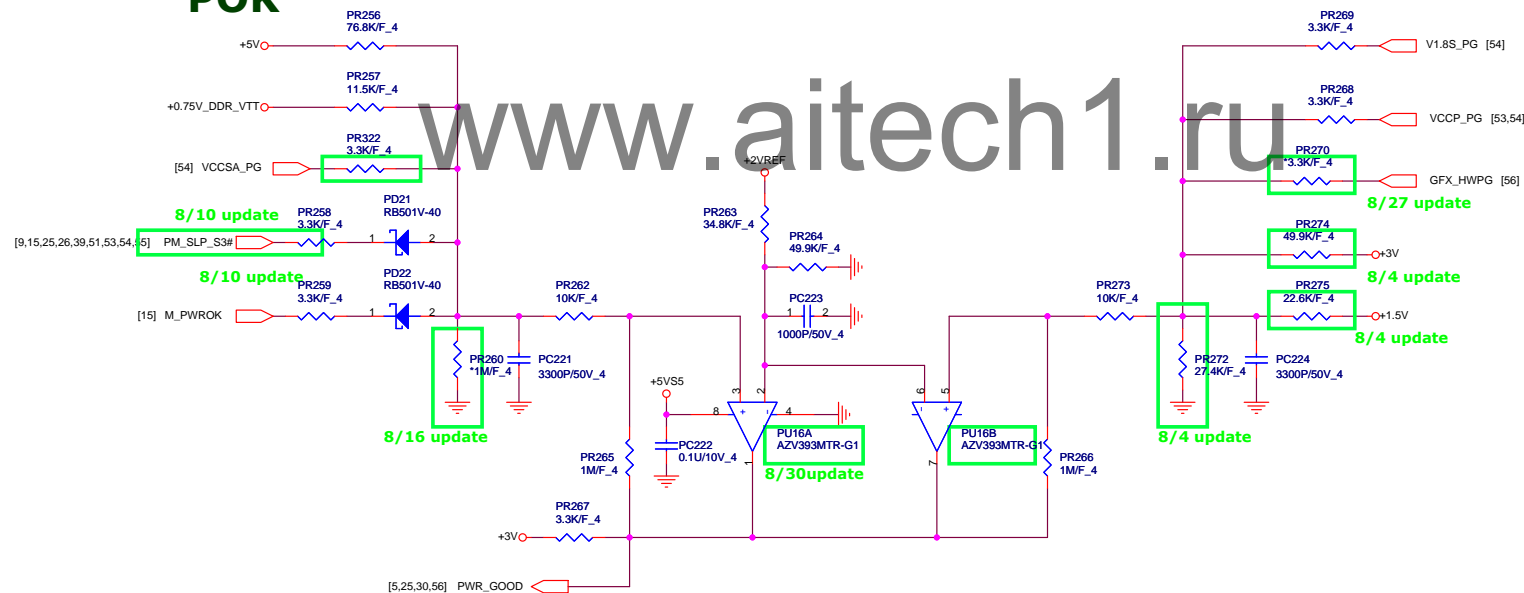
# POK CKT

```
PM_SLP_S4# = SUSON
PM_SLP_S3# = MAINON
+V5S = +5V
+V3S = +3V
+V0.75S = +0.75V_DDR_VTT
```

## For iAMT

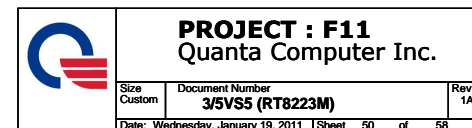


**POK**

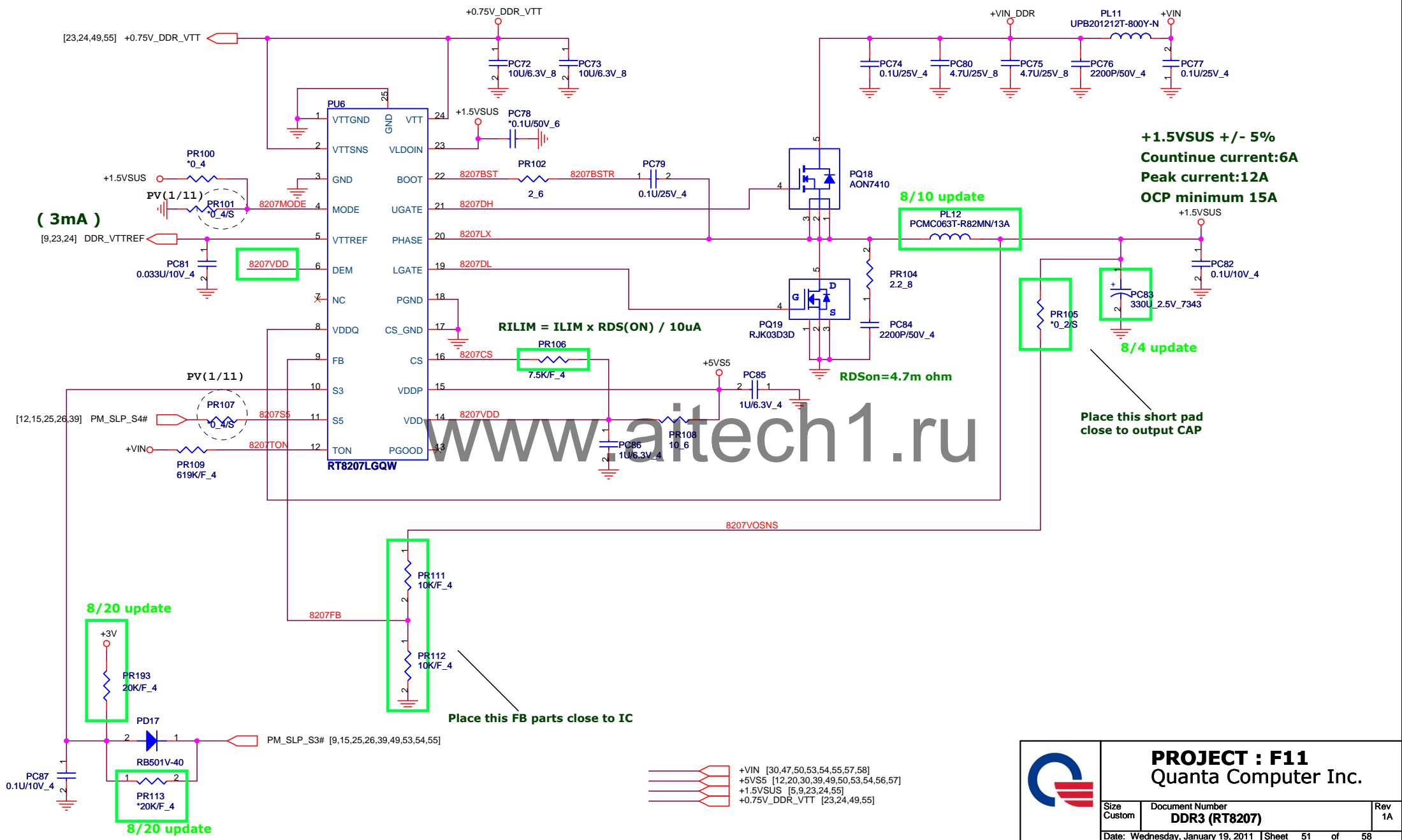


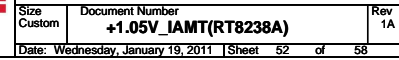
**PROJECT : F11**  
Quanta Computer Inc.

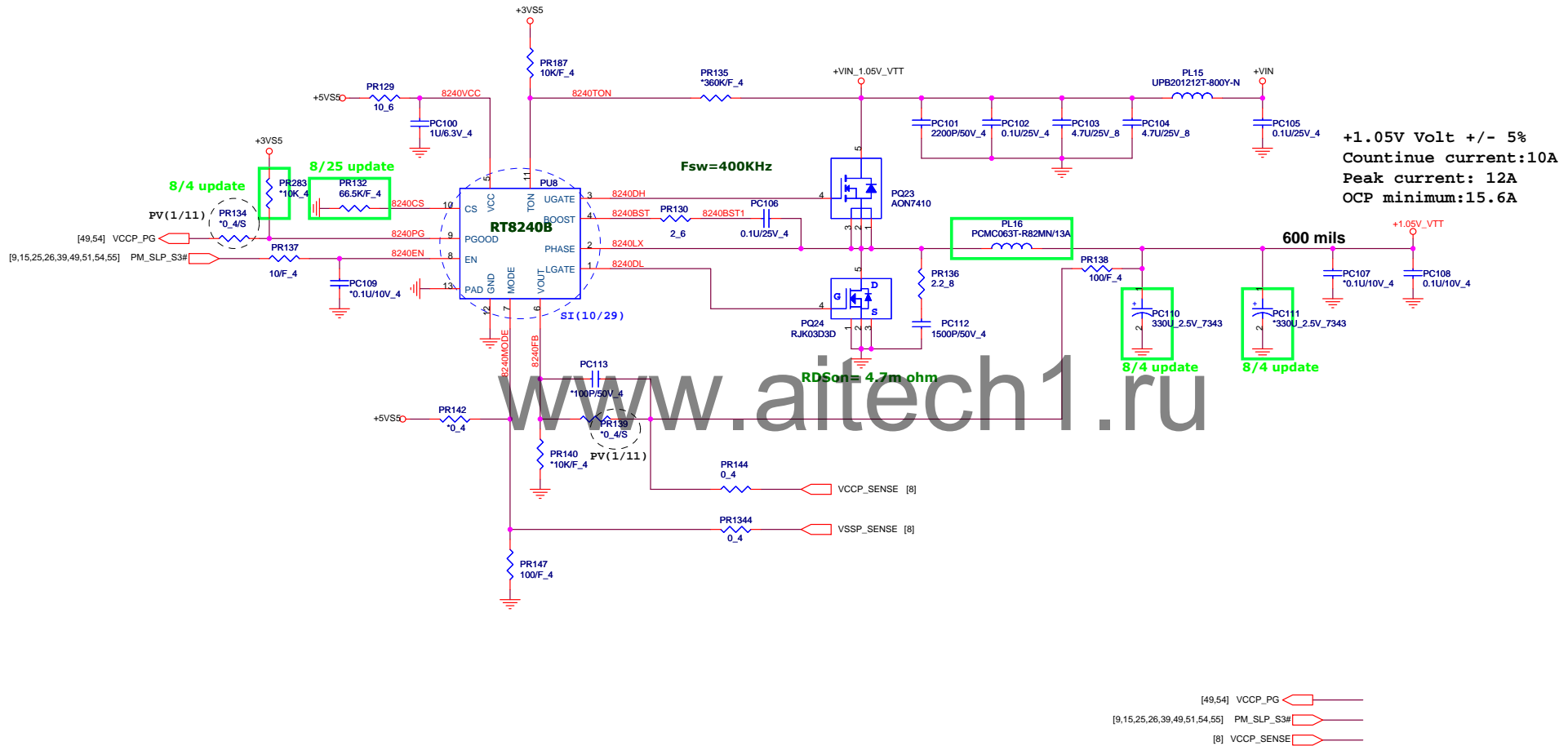
Size Custom	Document Number <b>CHARGERII</b>	Rev 1A
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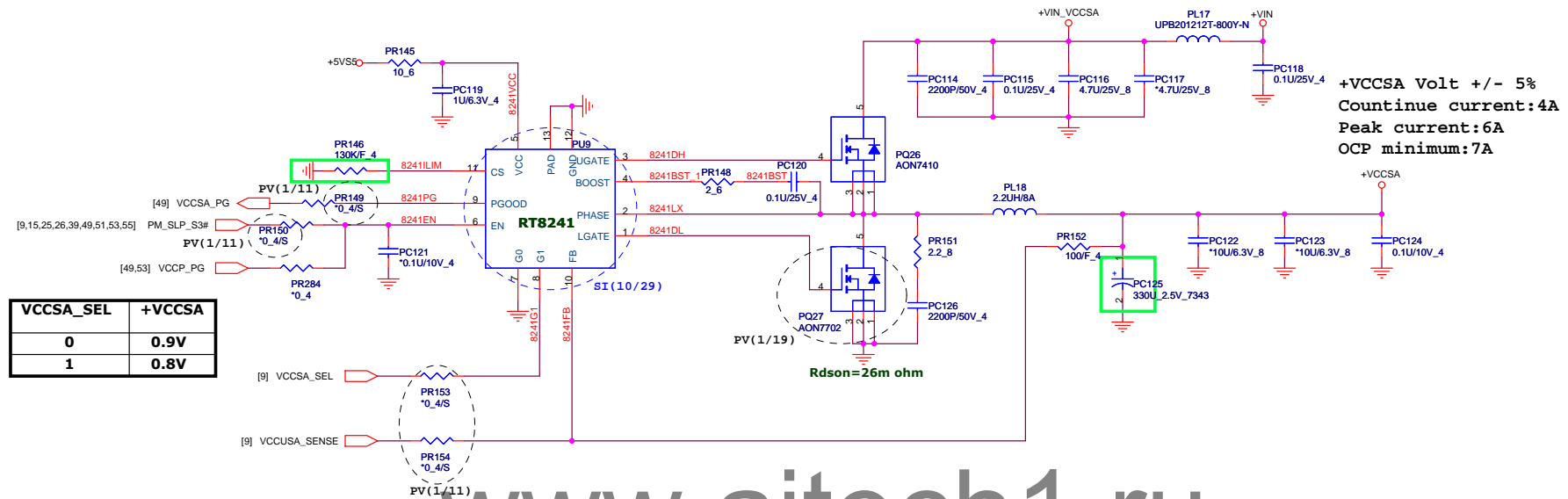


( VTT/2A )



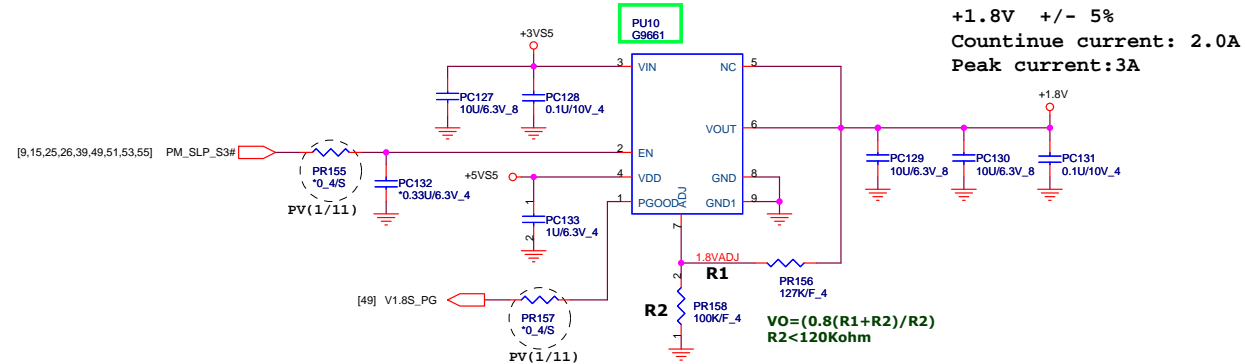






+VCCSA Volt +/- 5%  
 Countinue current:4A  
 Peak current:6A  
 OCP minimum:7A

11/4 SI change



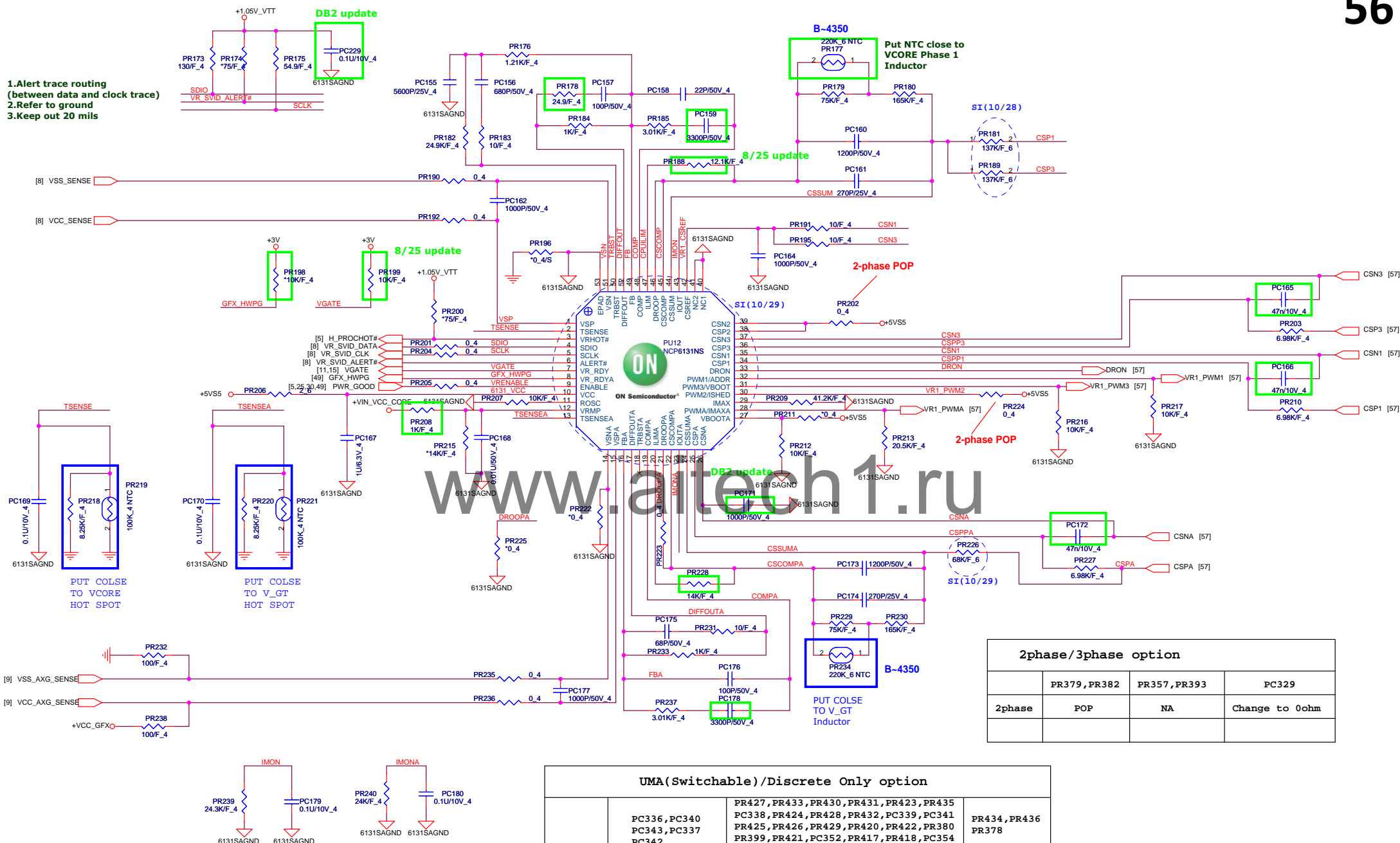
+1.8V +/- 5%  
 Countinue current: 2.0A  
 Peak current:3A

$$VO = (0.8(R1+R2)/R2)$$

$$R2 < 120Kohm$$

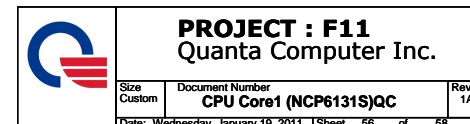


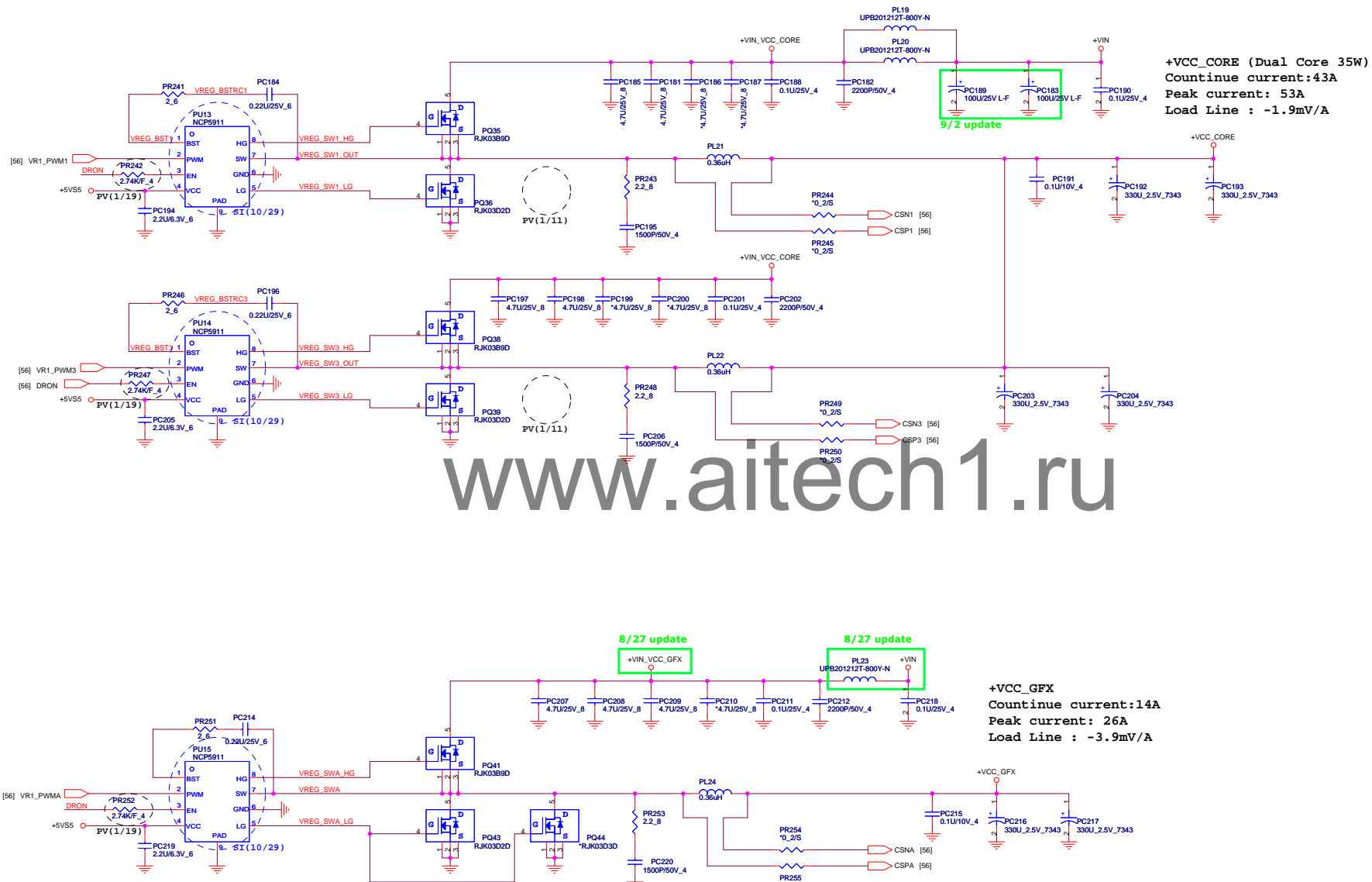
- 1.Alert trace routing  
(between data and clock trace)
- 2.Refer to ground
- 3.Keep out 20 mils



2phase/3phase option			
	PR379,PR382	PR357,PR393	PC329
2phase	POP	NA	Change to 0ohm

UMA(Switchable)/Discrete Only option			
	PC336,PC340 PC343,PC337 PC342	PR427,PR433,PR430,PR431,PR423,PR435 PC338,PR424,PR428,PR432,PC339,PC341 PR425,PR426,PR429,PR420,PR422,PR380 PR399,PR421,PC352,PR417,PR418,PC354 PC419	PR434,PR436 PR378
UMA	POP	POP	NA
Discrete	Change to 0 ohm	NA	POP





**PROJECT : F11**  
 Quanta Computer Inc.

Size C	Document Number <b>CPU Core2 (NCP5911)QC</b>	Rev 1A
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